

CSE3215 Embedded Systems Laboratory

Lab6 – Mini Project

The objective of the mini-project is to develop a peripheral device that will be interfaced through a serial peripheral interface (SPI) to the HCS12. SPI is a synchronous serial communications link that can be used to communicate with external peripherals at high speeds.

Your peripheral must include status and data registers that can be both written to and read from the microcontroller. It must be implemented in Verilog on the Altera DE2 board and be of your own design and implementation.

Your grade out of 20 will be assessed as follows:

5 Marks: Specification and interface. A complete description of the interface to be developed and the functionality of the peripheral are required. This includes all registers, operating mode, specifications on performance, capacity, function and other relevant parameters. The circuit must be implementable in the Altera DE2 and any additional hardware required must be specified fully *including cabling or connections between the devices*. Take care to keep the document clear and concise.

Specification document is due March, 12, 2012. No group may start the lab without an approved specification.

10 Marks: Demo and implementation. Demos will be scheduled in the last hour of the final lab session. Demos consist of a five-minute presentation of the system and demonstration in the lab setting. Program/design documentation should be complete (code should be well documented and submitted electronically on Prism within 24 hours of the demo). Also, include an annotated trace of the SPI signals using the logic analyzer during a transmission.

5 Marks: Data Sheet. Create a datasheet for your SPI peripheral (many examples, i.e., <http://www.alldatasheet.com/view.jsp?Searchword=CAT28C162S16A-25TE13>). Your datasheet should include features, description, interfacing, timing diagrams, example applications and operation. You **do not** need to specify package type, ordering information, electrical or thermal ratings of the device (these will follow the Altera chip) but do need to fully describe pins used, signals and so on.

Reference Reading (you will likely need to look beyond this)

Dragon12 Schematics
Dragon12 Schematics.pdf

SPI Block Users Guide
S12SPIV2.pdf

Altera DE2 User Manual
DE2_UserManual.pdf
DE2_schematics.pdf
cyc2_cii5v1_01.pdf (Cyclone II family data sheet)

Hint: You can restrict your interface to a particular SPI mode (i.e. the Dragon12 to operate in master mode with the Altera as the slave using the CPHA = 1 transfer format).