

CSE 3201 Digital Logic Laboratory

Lab 3: Seven Segment Displays

Objective

The objective of this lab is to gain experience using the seven-segment displays that we will use in later labs.

Reference Material

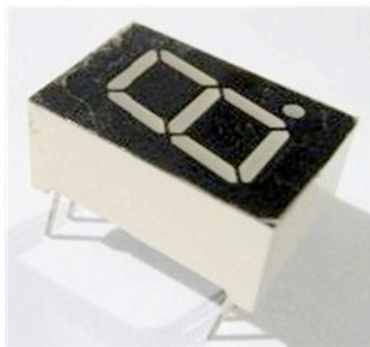
Altera DE2 manual and tutorial, available from the course web site.

Pre-Lab

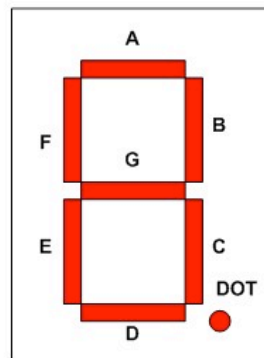
Background:

Seven segment LED displays are simple but effective and inexpensive information displays used in many embedded systems. Each display consists of an array of LEDs arranged in a pattern. When current flows through the diode it is illuminated. Typically, each diode is controlled by a single bit and either all the anodes or all the cathodes are tied together.

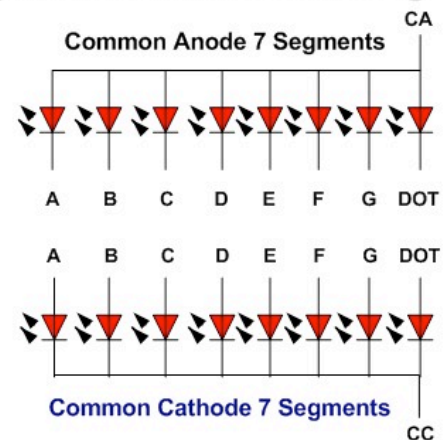
<http://www.ermicro.com/blog>



Typical 7 Segments Display



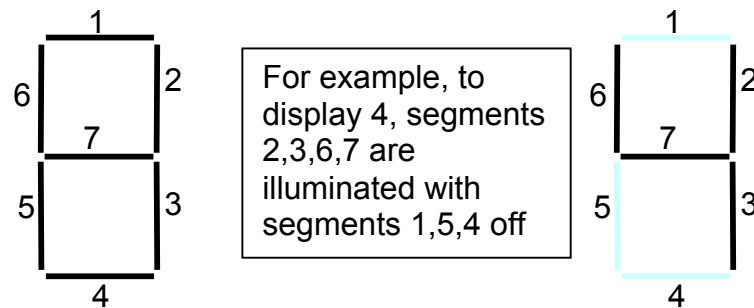
The 7 Segment's Name and the DOT



Common Cathode 7 Segments

The Seven Segments Display

To use the display, combinations of LEDs are switched on and off to represent a desired number. For example to represent the number 4, LEDs number 2,3,6 and 7 are ON the rest are off.



1. Design a circuit that displays, on one of the seven segments displays, the hex representation (0 to 9 plus A, B, C, D, E, and F) for the binary number represented by the set of switches SW0 to SW3. For example if SW3 SW2 SW1 SW0 are 0100 (4) the 7-segment display should display the number 4, if they are 1110 then E should be displayed. Note that a segment is illuminated by driving it with logic 0 (that is it is active low).
2. Construct a truth table (4 inputs, 7 outputs, 16 rows) to show the relation between the switches and the LEDs.
3. Use the K-map method to minimize the combinational circuit. The tables and maps have to be ready before you start the lab. Look to see if there are opportunities for sharing of terms.
4. Design a Verilog implementation of this circuit using AND and OR gate primitives.
5. For the 'Bonus' also implement a behavioural version of the circuit.
6. Simulate your design.

Before entering the lab ensure that for each design you have at a minimum:

- Truth tables, Boolean expressions and other design aids.
- Fully documented Verilog source
- Test patterns and/or a testing strategy

If you are not prepared for the lab you will not be allowed to start. The two-hour lab time slots are strictly enforced and you must be prepared in order to complete the lab in the allotted time.

In Lab Procedure

1. Test your design on the board. Remember to assign the pins appropriately. Program the chip and verify that your circuit works.
2. Verify that the circuit works correctly. Demonstrate your design to the TA when you are satisfied it is correctly working.
3. If want to try the bonus repeat step one for your alternate design. For the report briefly compare the costs/benefits of the two designs.

The implemented circuits must be demonstrated to the TA who will note a completed lab and ask questions about your design. When implementing the circuit be sure to use the switches and lights to make it easy to demonstrate your circuits.

Evaluation

Lab demonstration, in-lab explanations and answers, debug and test approach.