CSE 3201 Digital Logic Laboratory

Lab6: Timing Measurements

Objective

The objective of this lab is to gain experience in measuring time relationships within your circuits using simulation, internal instrumentation and external measurement tools.

Reference Material

Altera DE2 timing simulation and Signal Tap tutorials. These are available from the laboratory section of the course wiki

You will also need your multiplier designs (fully functional) from lab 5. If you could not get lab 5 to work you can debug it now or borrow it from another group. **Clearly acknowledging who wrote the Verilog code and that it was used with their permission**. As always, use of circuits and code developed by others without proper attribution is academic fraud and will be treated as such. Ask if you are unsure about how to properly attribute another's work.

Pre-Lab

1. Look over the Signal Tap and Timing Simulation tutorials provided by Altera. If possible attempt these before the lab.

Lab

1. Create a timing simulation for your first multiplier circuit in part A of lab 5. Simulate for input A constant at 0xFF and input B counting from 0x79 through 0x85. Also simulate the converse (input B constant at 0xFF and input A counting from 0x79 through 0x85). Hint: there is a way to specify a count through the user interface and remember to make sure you keep the inputs stable for > 50 ns). Demonstrate your simulation to the TA and explain what you are seeing.
2. Create a SignalTap file to monitor your inputs and outputs. Use the clock50 signal (or the equivalent pin in the pin assignment) for the sampling clock. Set input A to 0xFF and input B to 0x80. Trigger the capture on the rising edge of bit 0 on input B. Repeat for input B set to 0xFF and input A transitioning from 0x80 to 0x81. Do the signals on the traces match your simulation? Why or why not?
3. Measure the relationship between SW[0] and LED[15] on the oscilloscope. Route these signals out to GPIO pins configured as outputs in Verilog (i.e.

with an assign). Measure the delay between a transition on SW[0] and stable output on LED[15]. Does it match Q1 or Q2?

4. Bonus repeat part 1 and 3 for the circuit in Part B of lab 5.