CSE 3201 Digital Logic Laboratory

Lab8: Counters and Registers

Objective

The objective of this lab is to gain experience with counters and shift registers.

Pre-Lab

A)

1. Create 3 different designs for a 4-bit counter
    a. An asynchronous counter based on T flip-flops.
    b. A RTL design based on addition and non-blocking assignments.
    c. Using the lpm counter module from Altera.
2. Simulate your designs.
3. Compare the implementations in terms of maximum frequency and resources used.

B)

Design a 5-bit linear feedback shift register circuit. The circuit is a standard 5-bit shift right register (see figure 5.17) except that the input to the first stage should be $Q_2 \oplus Q_n$ rather than simply Q_n. Include in your circuit an asynchronous preset and a parallel load capability. The output of the circuit Q_n is an unpredictable bit stream often used in test equipment and communications.

- Determine how often the count repeats in simulation. What is the maximum frequency?

Lab

1. Download and test your counter circuits using one of the pushbuttons as the clock input.
2. Create a circuit with two 4-bit counters. Clock the first counter with the 50MHz clock on the DE2 board. Clock the second counter with the most significant bit of the first counter.
3. Using SignalTap measure the frequency of the counting of the second counter. How often does it overflow? Demonstrate completion to the TA.
4. Download and test your LFSR circuit. Does the pattern ever repeat? How often? Are there any problematic count states?

The implemented circuits must be demonstrated to the TA who will note a completed lab and ask questions about your design. When implementing the circuit be sure to use the instruments (oscilloscope, SignalTap, simulation) switches and lights to make it easy to demonstrate your circuits.

Evaluation

Lab demonstration, in-lab explanations and answers, debug and test approach.