Dept. of and Electrical Engineering & Computer Science
CSE4201 – Computer Architecture
HW 3
Due Nov. 19, 2013

Problem 3.15 from the text book

A direct mapped cache consists of 128 blocks each is 4 words. The main memory is 16K words. The time to transfer a cache line from the main memory to the cache is 200 nsec. The cache access time is 10 nsec. Assuming an initially empty cache.

a) Show the format of the memory address
b) If the program loops from location 20-200 10 times, how many misses?
c) If the program loops from location 20-100 10 times, how many misses?
d) Compute the effective address time for parts (b) and (c)

Problem given in the class