CSE4210 Architecture & Hardware for DSP

Chapter 1

Introduction

Instructor: Prof. Peter Lian
Department of Electrical Engineering & Computer Science
Lassonde School of Engineering
York University

CSE4210 Architecture & Hardware for DSP

- Instructor: Prof. Peter Lian
  email: peterlian@cse.yorku.ca
  tel: 416-736-2100 ext 44647
- Couse Web:
  https://wiki.cse.yorku.ca/course_archive/2013-14/W/4210/
- Schedule:
  - Lectures: Mon & Wed 13:00 – 14:30, Room CB120
  - Labs: Tue. 11:30 – 13:30, LAS 3057
- Office hours: Mon 14:30 – 16:00 @ LAS 1012C

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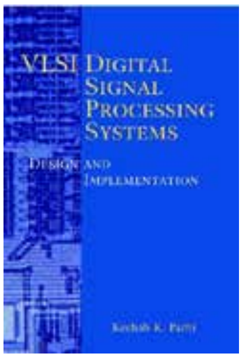
- Text book:
  VLSI Digital Signal Processing Systems: Design and Implementation
  by Keshab K. Parhi
  John Wiley & Sons
  ISBN 0-471-24186-5
  http://ca.wiley.com/WileyCDA/WileyTitle/productCd-0471241865.html



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- Assessment:
  - Quizzes: 15%
  - Project: 25%
  - Midterm test: 25%
  - Final exam: 35%

Topics

- Number systems
- Building blocks
- Algorithm representation
- Transformation (retiming, unfolding, folding)
- Mapping algorithms into hardware
- Low power design

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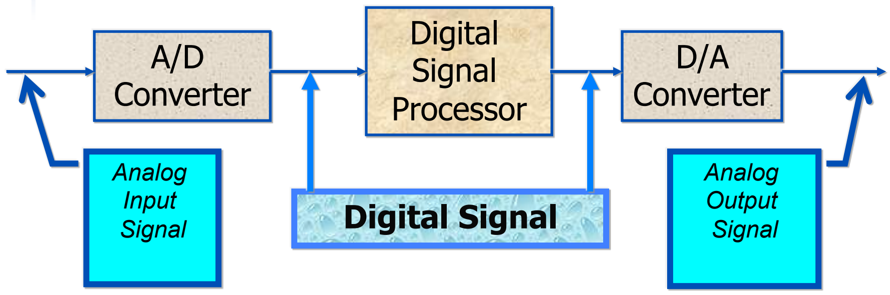
Digital Signal Processing

What is Digital Signal Processing ?

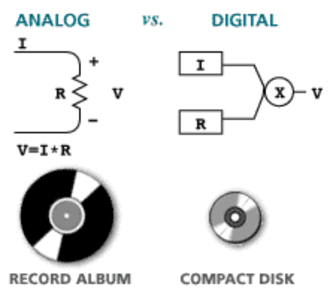
- Digital Signal Processing is concerned with the representation of signals in digital form, and with the processing of these signals and the information that they carry.



Advantages of DSP

Digital Hardware

- Can implement arbitrary nonlinear operations
- Is less sensitive to variations in environment
- Is programmable



Signal Processing Techniques

Signal-Analysis/Feature-Extraction :

extract useful information from a given signal

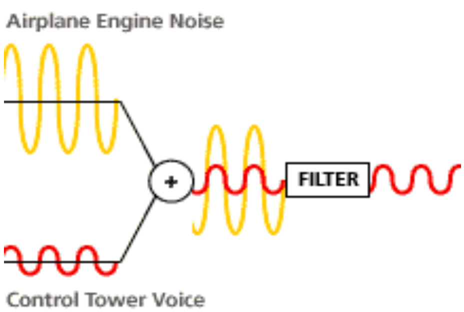
Examples :

speech recognition, location and identification of targets from sonar signals

Signal Filtering/Shaping Techniques

Improve the quality of a given signal

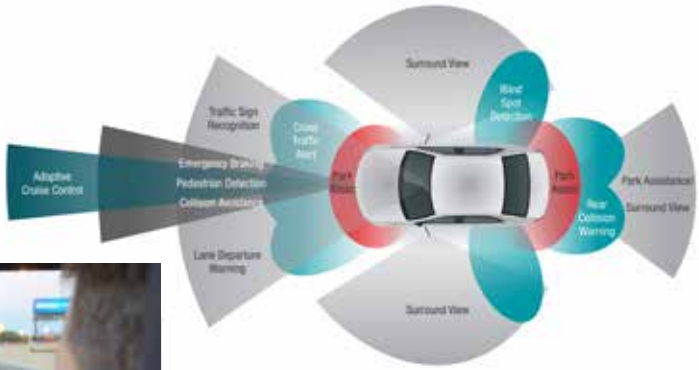
Examples: removal of noise and interference by frequency selective or statistical filtering, splitting of signal into simpler components.



Applications

- High quality digital audio system
- Digital TV, HDTV, 3D TV
- Wireless LAN, e.g. IEEE802.11a
- Mobile phone, e.g. CDMA, W-CDMA
- Medical instruments, e.g. ECG

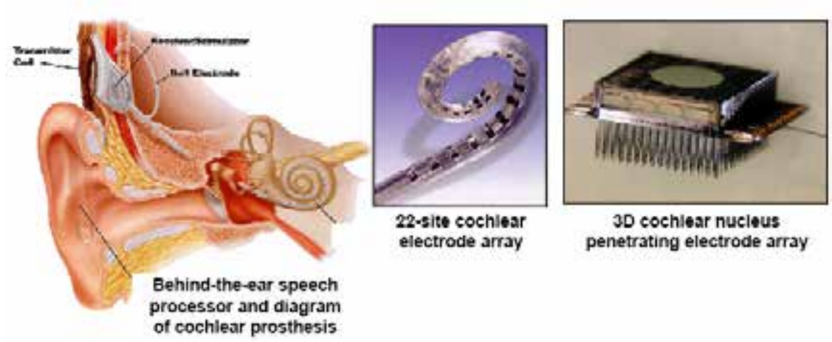
Application in Car



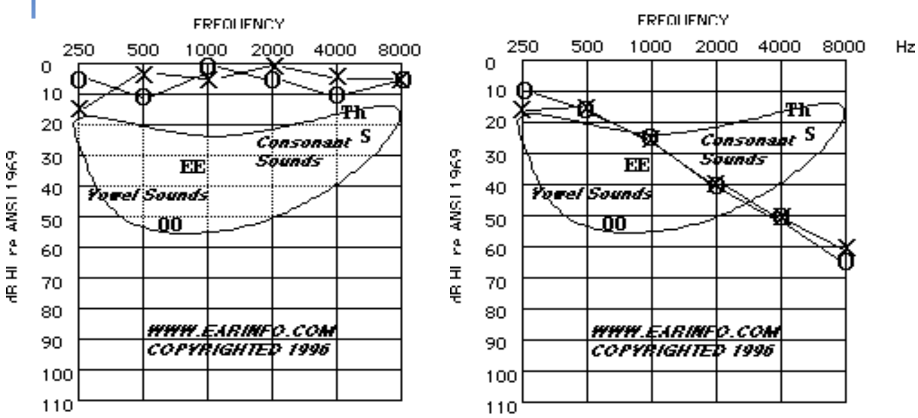
Audi A7 auto-piloted car at CES 2014

Bio-applications : Hearing Aid

- Cochlear Implants

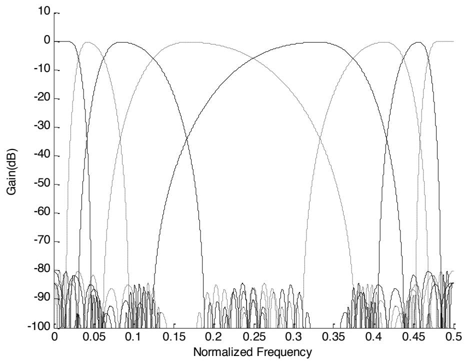


FIR Filter Bank for Hearing Aid

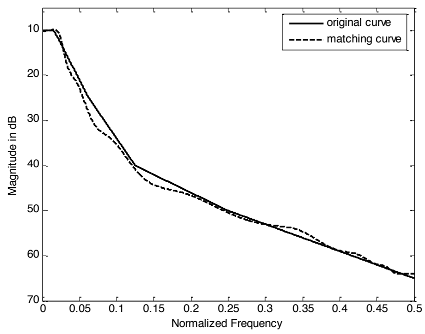


Examples of audiograms for (Left) normal hearing; (Right) presbycusis

8-band Non-Uniform Filter Bank

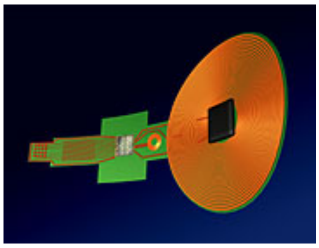


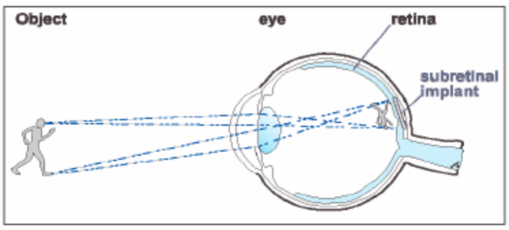
Frequency response
of filter bank



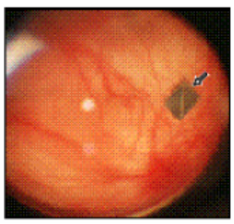
Matching for presbycusis

Bio-applications: Retinal Implants





Principle of subretinal implants

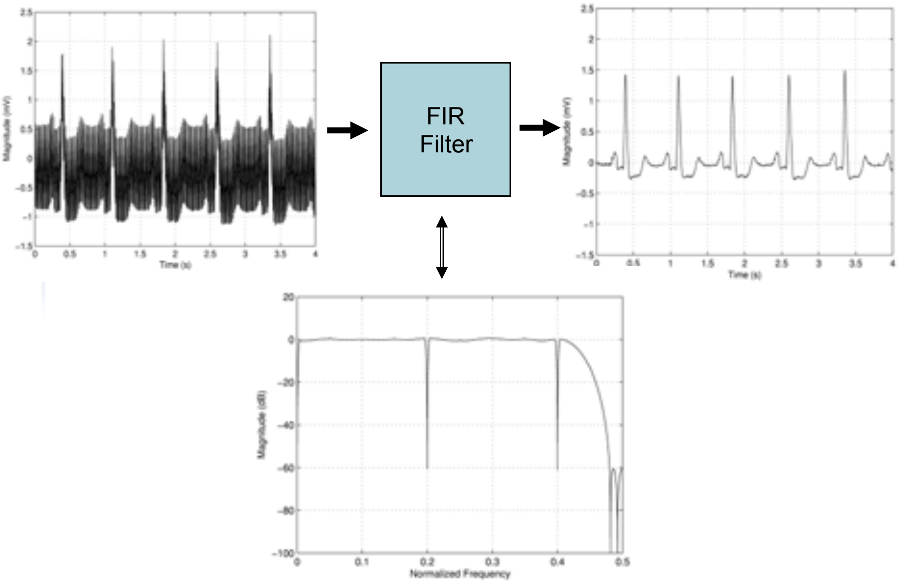


Chip implanted
into a rat's eye

Visual Cortical Stimulator

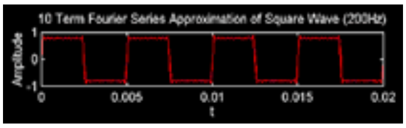
Biomedical Application: ECG

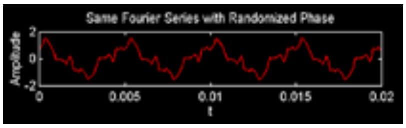
FIR Filtering for ECG Signal



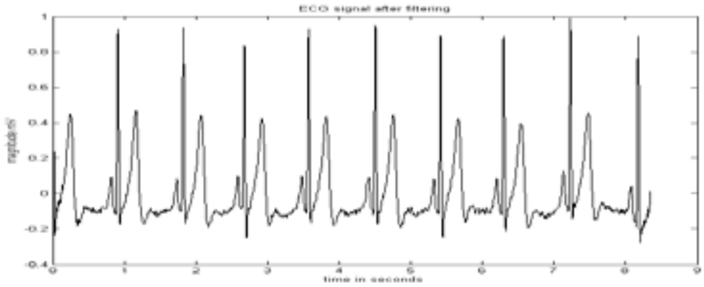
Linear Phase

- Audio signals.





- Electrocardiogram (ECG).



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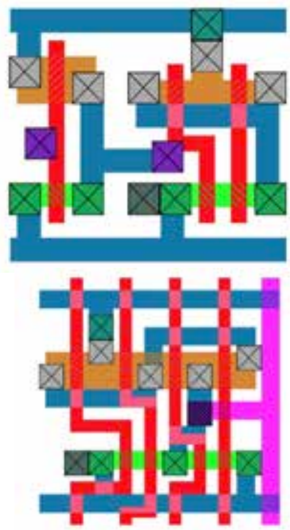
VLSI Design

Types of DSP

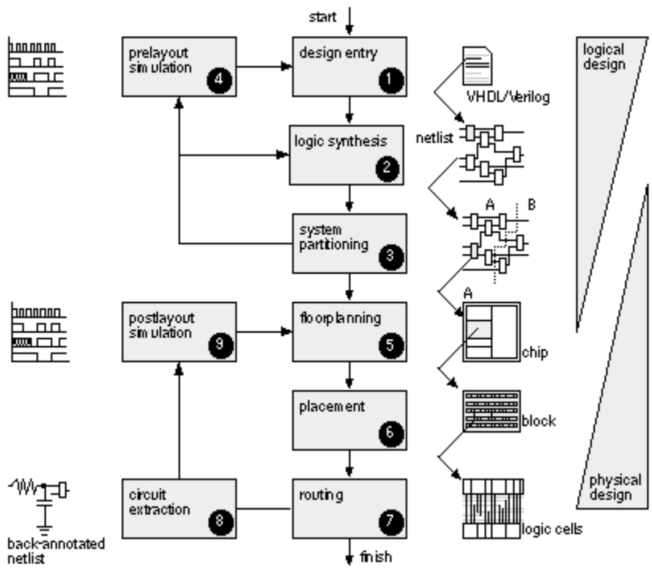
- General purpose DSP
  - Programmable
  - Fixed point and floating-point compute engine
  - Multicore, power optimized, ultra low power
  - Many suppliers in market
- Application specific DSP
  - Full-custom
  - Standard cell
  - Programmable, e.g. FPGA

Full Custom vs. Standard Cell

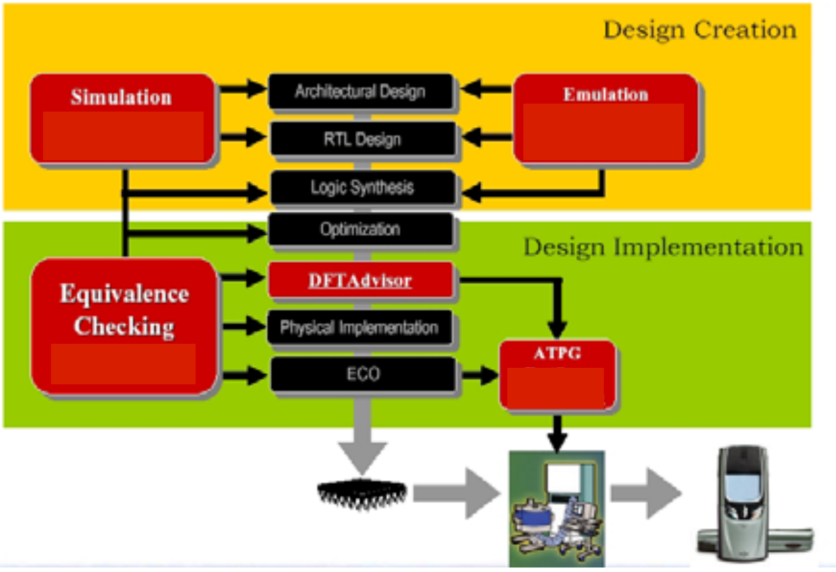
- Full custom
  - Analog/digital with all customized mask layers and some logic cells
  - Full control over sizing and layout
- Standard cell
  - Using pre-designed “cells”
  - Constant-height and regular pin locations



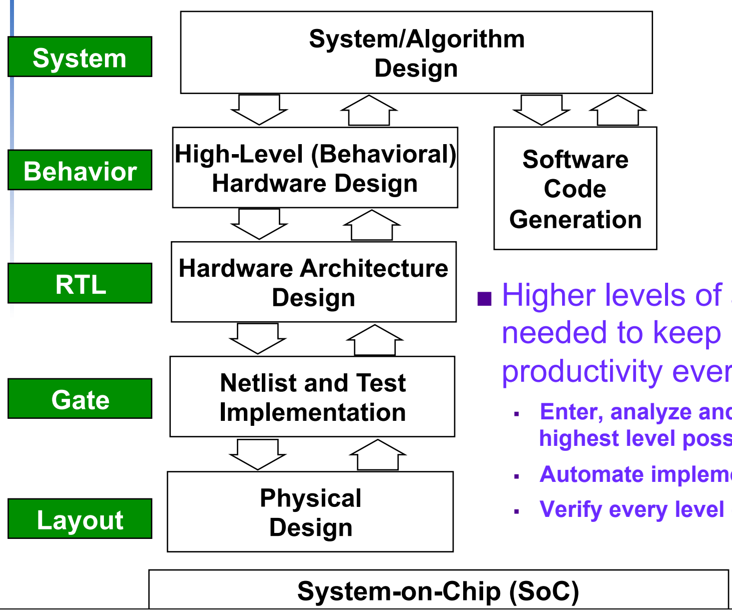
Cell Based Design Flow



Flow Chat



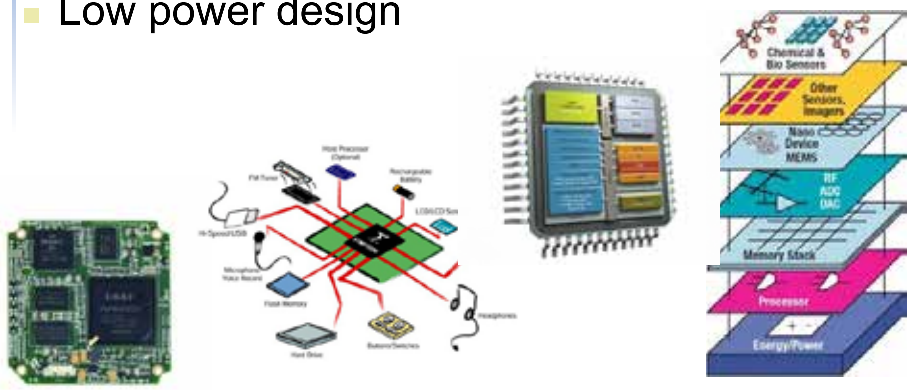
High Level Design Methodology



- Higher levels of abstraction needed to keep up with 10X productivity every 6 years
  - **Enter, analyze and validate at the highest level possible**
  - **Automate implementation**
  - **Verify every level of abstraction**

The Trend in VLSI Design

- System integration: moving from board to chip → System-on-Chip (SoC)→ System-in-Package → 3D IC
- Low power design



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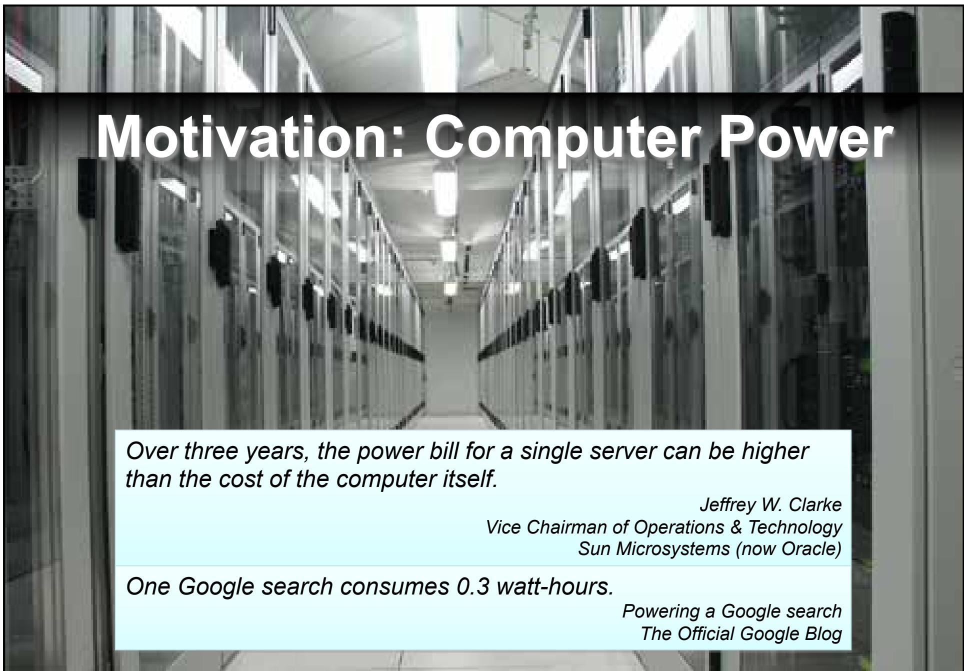
Why Low Power Design?

Motivation: Battery Life



Motivation: Computer Power

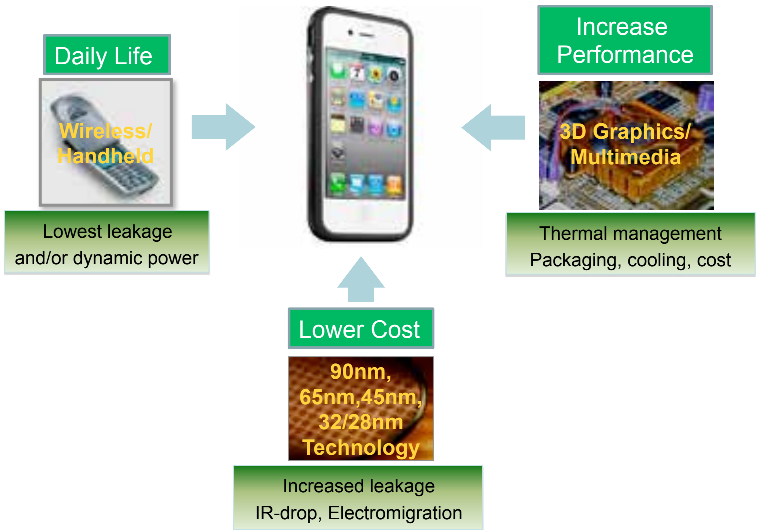
Over three years, the power bill for a single server can be higher than the cost of the computer itself.

Jeffrey W. Clarke
Vice Chairman of Operations & Technology
Sun Microsystems (now Oracle)

One Google search consumes 0.3 watt-hours.

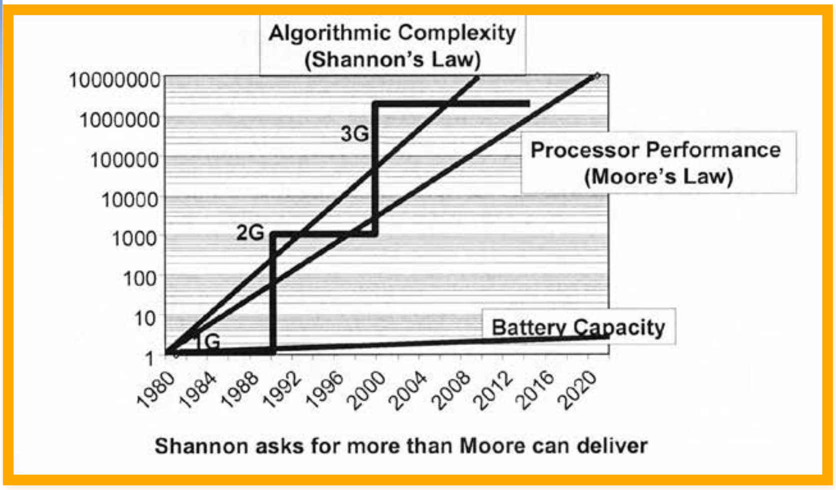
Powering a Google search
The Official Google Blog

The Performance vs. Power Dilemma

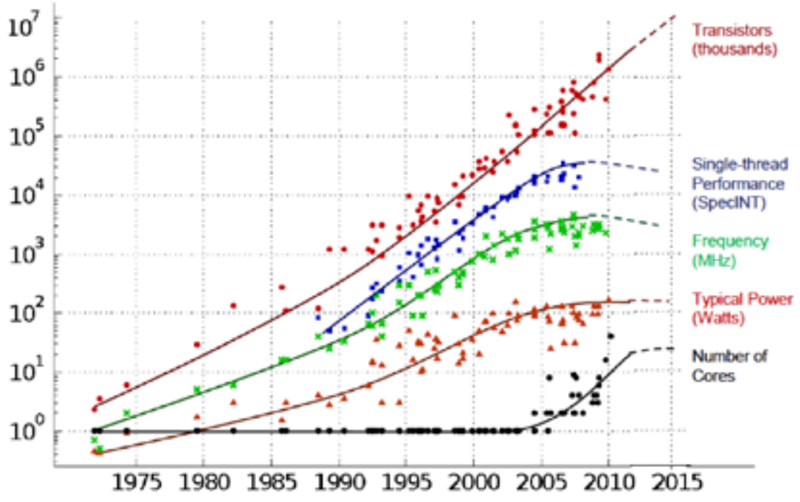


The Performance vs. Power Dilemma

- The algorithmic driving force →design complexity



Moore's Law - a Few to Billions in 50 Years

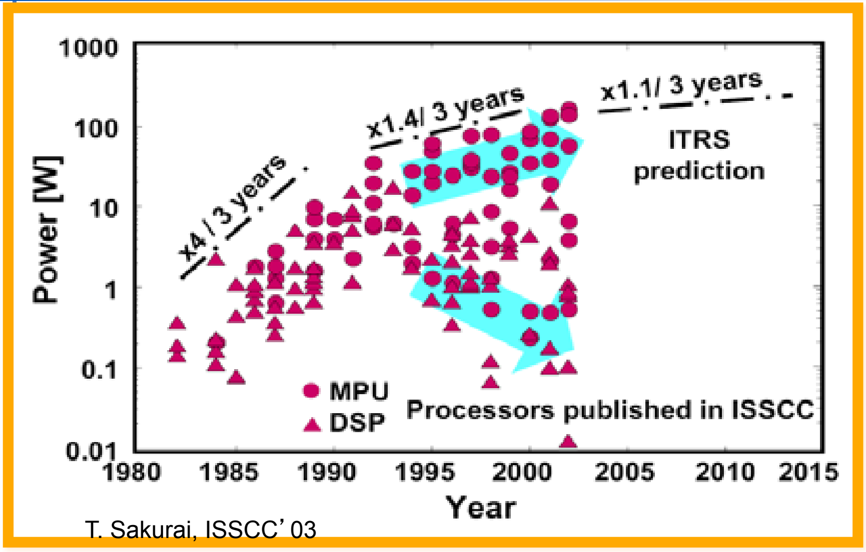


Original data collected and plotted by M. Horowitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond and C. Batten
Dotted line extrapolations by C. Moore

Increasing Performance

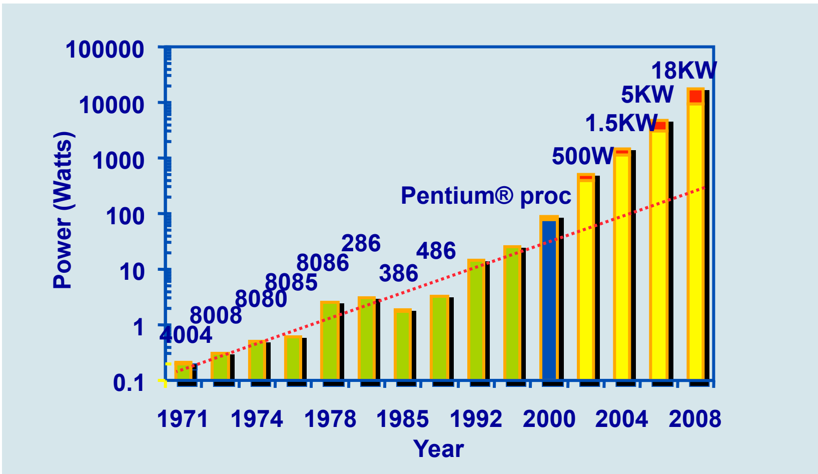
YEAR OF PRODUCTION	2003	2006		2009	2010	2011	2015
Process Technology (nm)	130	90		65	45	32/28	12
Supply Voltage (V)	1.2	1		0.8	0.6	0.5	0.3
Clock Frequency (MHz)	1000	2000		2500	2900	3200	4000
Application (maximum required performance) Application (other)	Still Image Processing Web Browser Electric Mailer Scheduler	Real Time Video Codec (MPEG4/CIF) TV Telephone (1:1) Voice Recognition (Input) Authentication(Crypto Engine)			Real Time Interpretation TV Telephone (>3:1) Voice Recognition (Operation)		
Processing Performance (GOPS)	0.3	2	14		77	461	2458
Required Average Power (W)	0.1	0.1	0.1	0.1	0.1	0.1	0.1
Required Standby Power (mW)	2	2	2		2	2	2
Battery Capacity (Wh/Kg)	120	200	200		400	400	400

The Power Crisis (1)



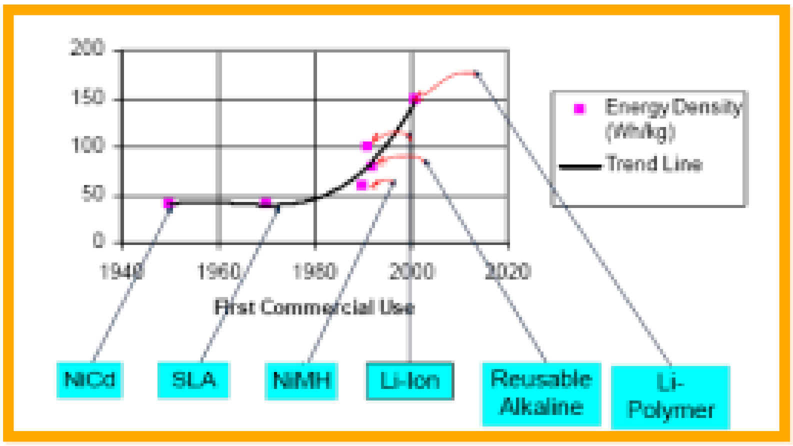
T. Sakurai, ISSCC'03

The Power Crisis (2)



Courtesy of Intel

The Battery Crisis (1)



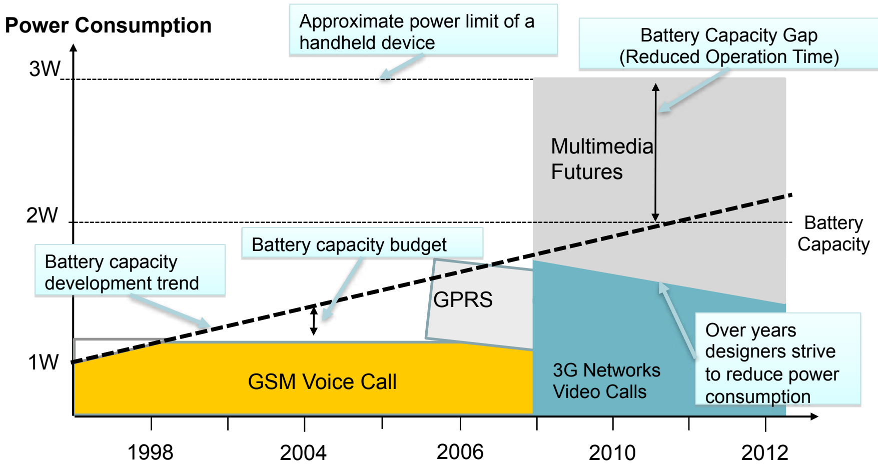
Factor of 4 over the last 30 years!

The Battery Crisis (2)

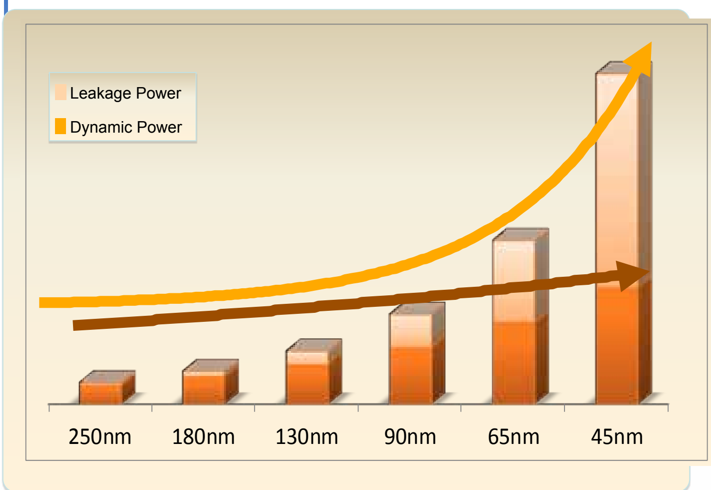
- **Little change in basic technology**
  - store energy using a chemical reaction
- **Battery capacity doubles every 10 years**
- **Energy density/ size, safe handling are limiting factor**

Energy density of material	***KWH/kg***
Gasoline	14
Lead-Acid	0.04
Li polymer	0.15

Power Consumption & Battery Capacity Trends



Ratio of Dynamic and Leakage Powers



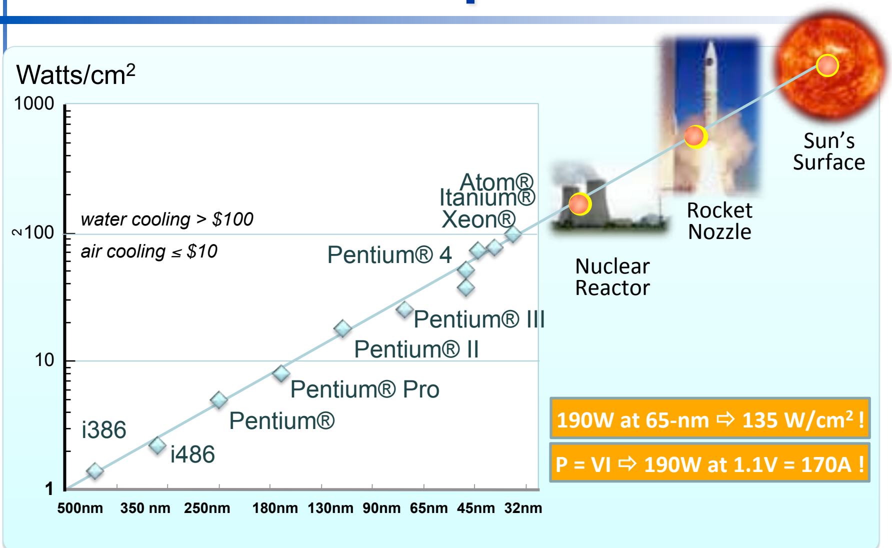
Leakage power grows from 40-50% of power budget at 90 nanometer to 50-60% at 65nm and beyond.

Importance of Standby Power

Of the $250 billion spent globally each year powering computers, about 85% of that energy is simply wasted idling.

Source: Economist, August 11, 2010

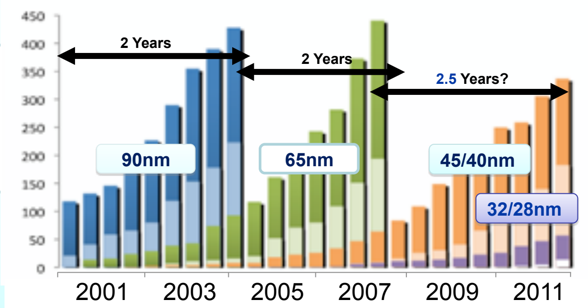
Power Consumption Trends



Technology Scaling Continues

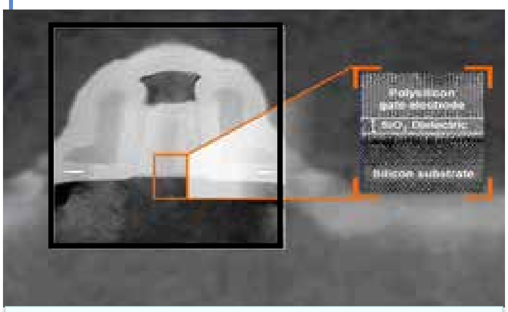
Device sizes are still scaling

Cost/device is still scaling down. This is what is driving scaling.



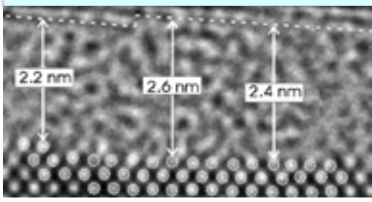
- Voltages are not scaling very fast
  - Threshold voltages set by leakage
  - Gate oxide thickness is set by leakage
- Now Vdd and Vth are set by optimization

Leakage Sources

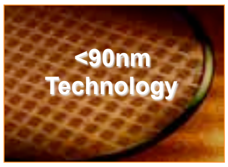


3 to 5 Molecules Of SiO_2 Dielectric

±1 Molecule Makes The Difference



Power Affected Problems

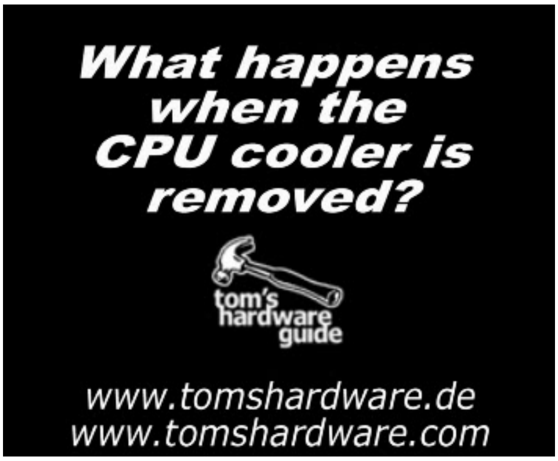
	Low Power	Power Efficiency	Reliability
			
Application	• Wireless • Handheld • Embedded systems	• Microprocessors • Graphics/multimedia • Networking/telecom	• All design<90nm
Concern	• Battery life • Leakage power • Dynamic power	• Thermal management • Packaging, cooling cost	• Leakage power • IR-drop • Electromigration

The Signs of Crisis Are Visible

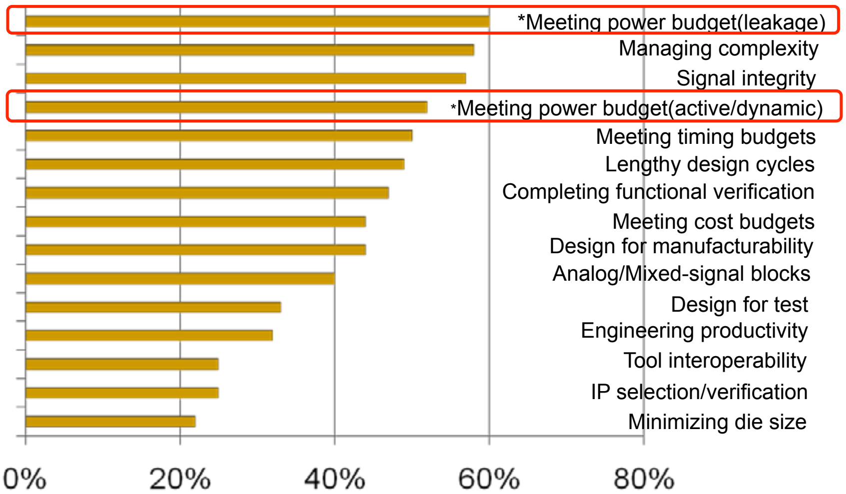
Voltage Is Breaking the Rules of Scaling

Source: ITRS 2005	90nm	65nm	45nm	32/28nm
Device Length (nm) ➲	1x	0.7x	0.5x	0.3x
Delay (ps) ➲	1x	0.7x	0.5x	03x
Frequency (GHz) ⇨	1x	1.43x	2x	3x
Integration Capacity (BT) ⇨	1x	2x	4x	8x
Capacitance (fF) ➲	1x	0.7x	0.5x	0.3x
Die Size (mm^2)	1x	1x	1x	1x
Voltage (V) ➸	1x	0.85x	0.7x	0.55x
$Power_{Dyn}$ (W) ➸	1x	>0.7x	>0.5x	>0.3x
Manufacturing (microcents/T) ➲	1x	0.35x	0.12x	0.08x
V_{TH} (V) ➸	1x	.85x	.7x	.55x
I_{OFF} (nA/um) ⇨⇨	1x	~3x	~9x	~22x
$Power_{Dyn}$ Density (W/cm^2) ⇨	1x	1.43x	2x	4x
$Power_{Leak}$ Density (W/cm^2) ⇨	1x	~2.5x	~6.5x	~13.5x
Power Density (W/cm^2) ⇨	1x	~2x	~4x	~8x
Cu Resistance (Ω) ⇨	1x	2x	4x	8x
Interconnect RC Delay (ps) ⇨	1x	~2x	~5x	~12x
Packaging (cents/pin) ➸	1x	0.86x	0.73x	0.58x
Test (nanocents/T)	1x	1x	1x	1x

The Thermal Crisis

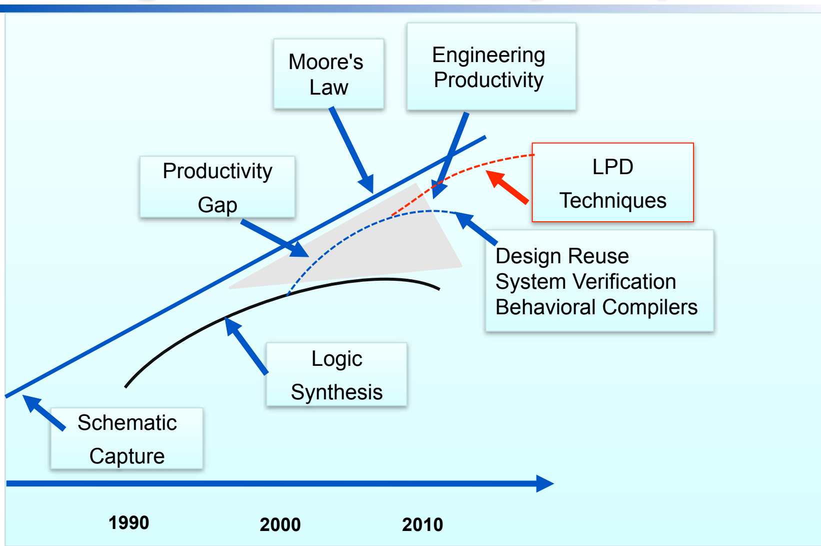


Significant Design Challenges

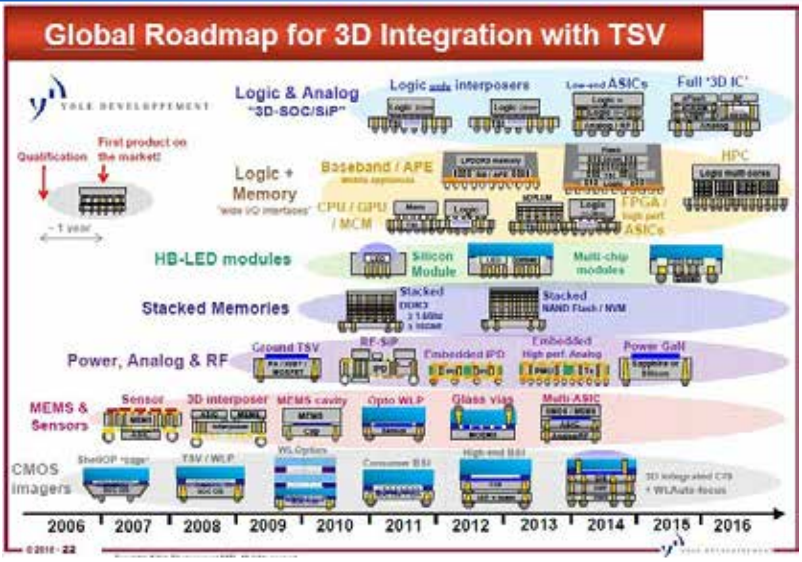


Survey results from large number of designers

Design-Productivity Gap



Design Complexity



The Importance of Low Power Design

- Battery life is limited by power.
- Cost for packaging and cooling increase rapidly with power dissipation
- Higher temperatures degrade performance and reliability
- Increasing integration increases power demand in portable applications
- Architecture is crucial in low power design