# CSE4210 – Architecture and Hardware for DSP

# Project Task 1

# Performance Comparison of Different Types of Adder

## *Introduction*

In Chapter 3, we introduced several types of adder including ripple-carry adder, carry-bypass adder, carry-select adder, and carry-lookahead adder. We learnt that the performance of an adder depends on the number of bits, architecture, and circuit implementation. In this task, you will design, simulate, synthesize, and verify several different types of adder. Then map these adders to Altera FPGA Cyclone II EP2C35F672C6 (DE-2 Development Board) for verification. Based on synthesis results, the performance of these adders will be evaluated in terms of speed (delay), area, and power.

You will use Altera Quartus II software for simulation and Altera DE-2 Development Board for verification. The Quartus software is available in LAS 3057. You can borrow the Altera DE-2 Development Board from the Lab Monitors at LAS 1006 during lab time (11:30am – 1:30pm). You need to return the board once the lab is over.

## *Tasks*

1. Develop Verilog codes for 8- and 16-bit ripple-carry adders, respectively, and a 16-bit square root carry-select adder. Assume the inputs are in 2's Complement format. Your adder should be able to handle overflow, i.e. to indicate there is an overflow.
2. Develop test benches for the functional verification of these adders.
3. Using Quartus II to perform your simulation and synthesis.
    a. Perform functional simulation to verify your designs.
    b. Map your design to Altera DE-2 development board, i.e. to select the target FPGA device that matches the DE-2 board.
    c. Perform timing analysis on your designs, considering the worst case. Record delays for each adder.
    d. From synthesis results, record area (gate counts) and power.
    e. Verify your designs by downloading your code to the DE-2 board and perform additions and subtractions.

4. Compare the performance of these adders in terms of speed, power, and area.
    a. Compare the delay, area, and power of 8 and 16 bits ripple-carry adder.
    b. Compare the delay, area, and power of 16-bit ripple-carry adder and Carry-Select adder.

## *Report*

Please include the following items in your report.

1. A brief introduction of the tasks.
2. Design procedures.
3. Simulation results, verification, and comparison figures or tables.
4. Conclusion
5. Appendix including Verilog code, test benches, and compilation reports.

### *Resource*

1. Tutorials and labs on Quartus II are available at:
http://www.altera.com/education/univ/materials/digital_logic/labs/unv-labs.html
2. A introduction on overflow detection can be found at:
http://www.cs.umd.edu/class/sum2003/cmsc311/Notes/Comb/overflow.html