EECS 3201: Digital Logic Design Lecture 15
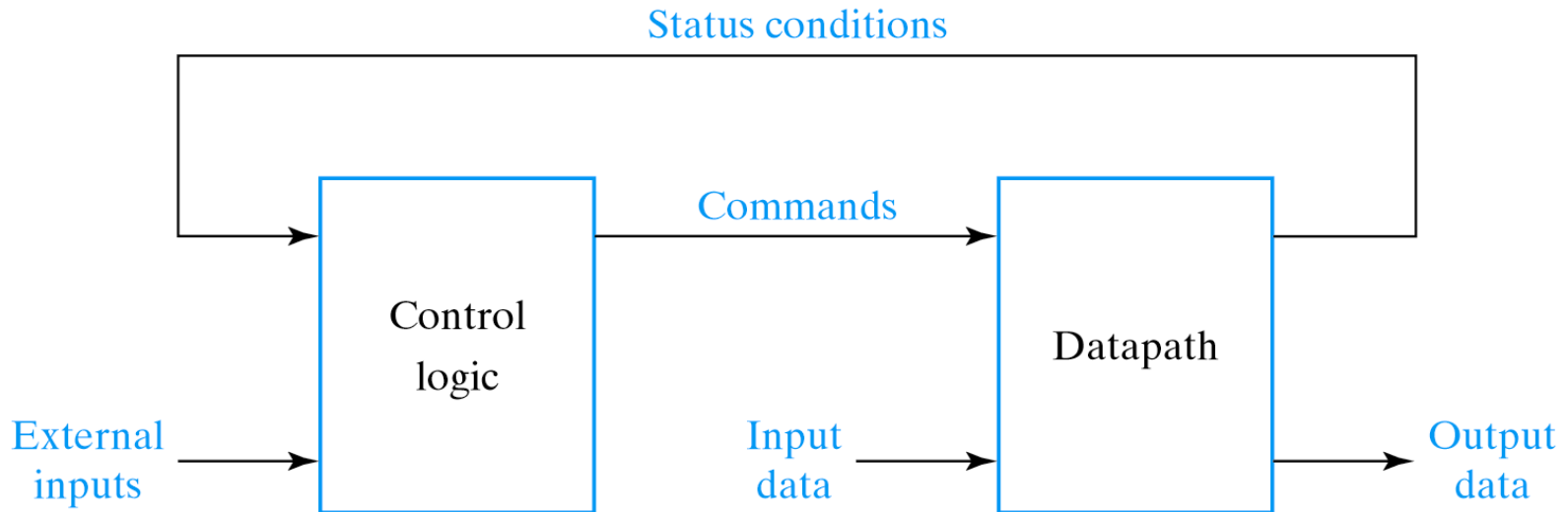
Ihab Amer, PhD, SMIEEE, P.Eng.
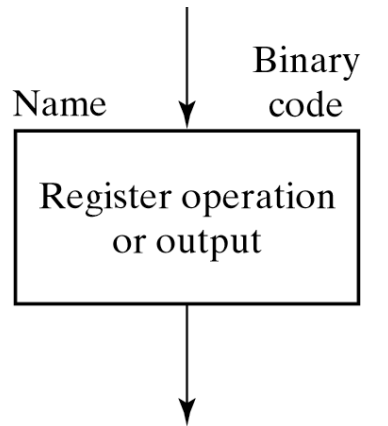
Structure of a Typical Digital System
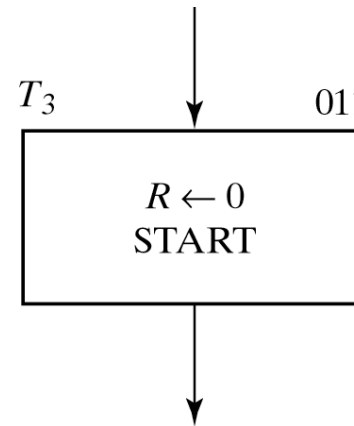

Control and Datapath Interaction

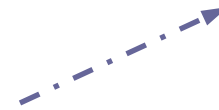# Elements Used in ASM Charts (1/2)

State Box

Name / Binary code

Register operation or output

(a) General description

T_3 / 011

$R \leftarrow 0$
START

(b) Specific example

Decision Box

0 — Condition — 1
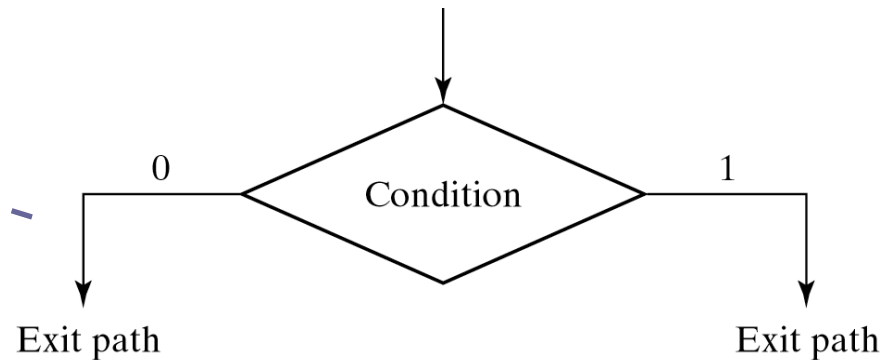
Exit path   Exit path

Elements Used in ASM Charts (2/2)

Conditional Box

From exit path of decision box

Register operation
or output

(a) General description

T_1 001

START

0   E 1

$R \leftarrow 0$

T_2 010

$F \leftarrow E$
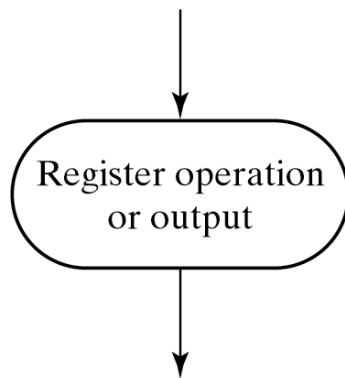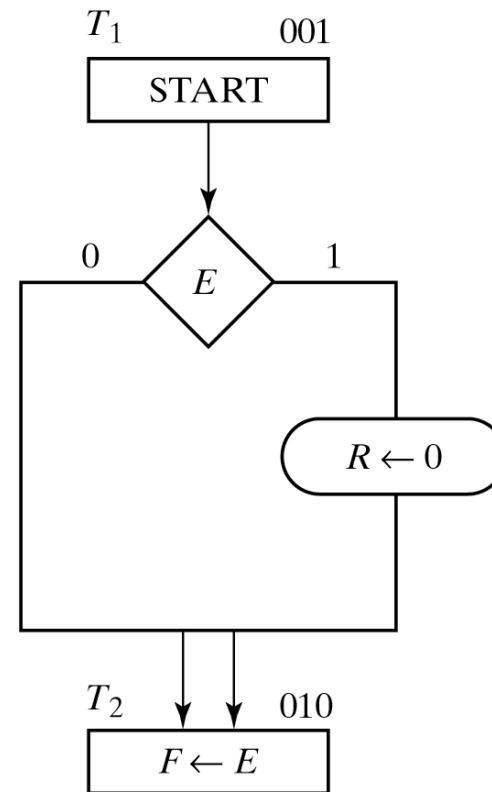
(b) Example with conditional box

Design with MUXs

- When binary assignment is used, the sequential circuit of a control unit typically consist of: flip-flops, decoder, and logic gates.
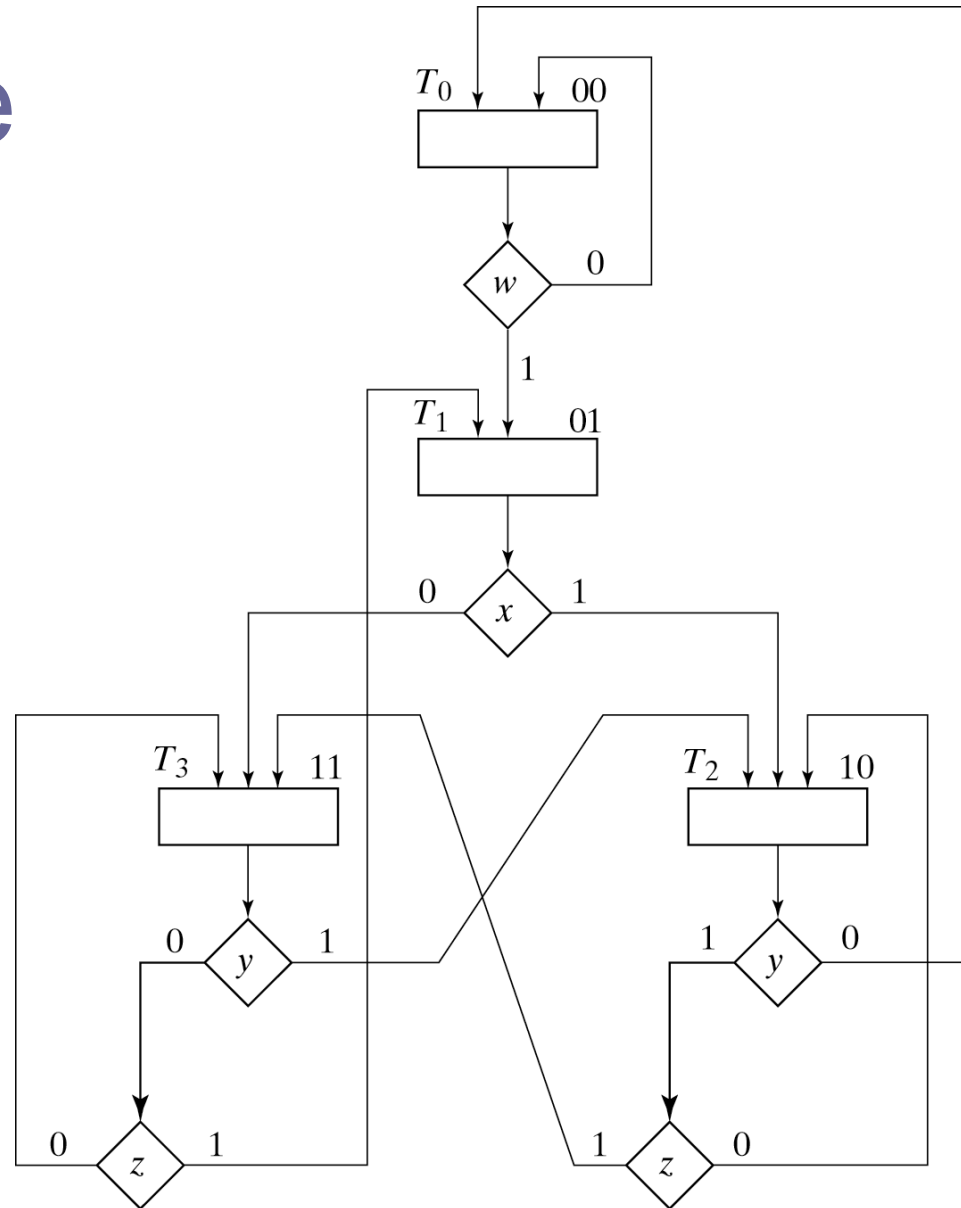- Replacing the gates with MUXs results in a regular pattern of 3 levels of components:
  - MUXs that determine the next state
  - Flip-flops that hold the present binary state
  - Decoder that provide a separate o/p for each state
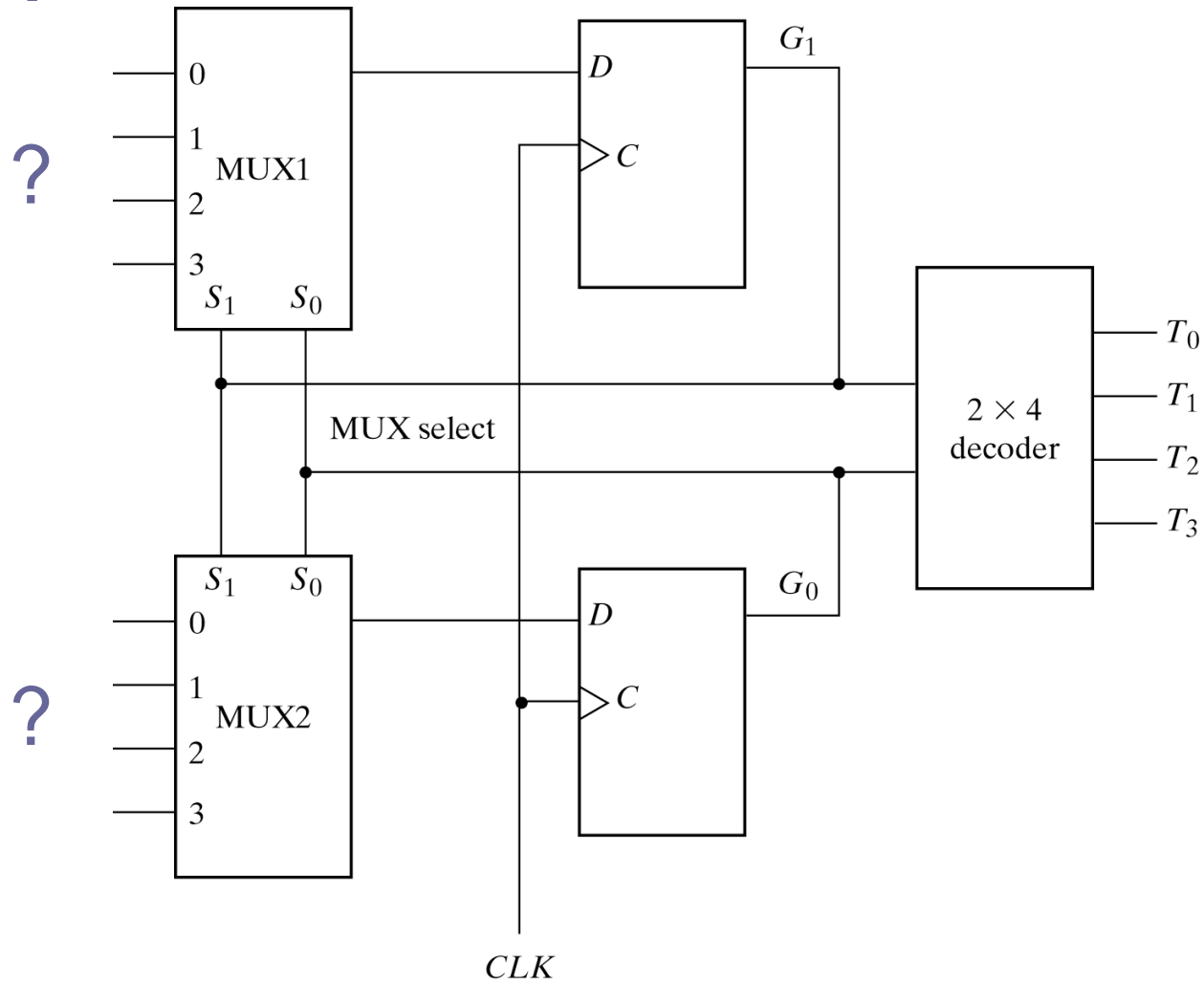- These 3 types of components are pre-defined standard cells in many ICs

Example
(1/4)

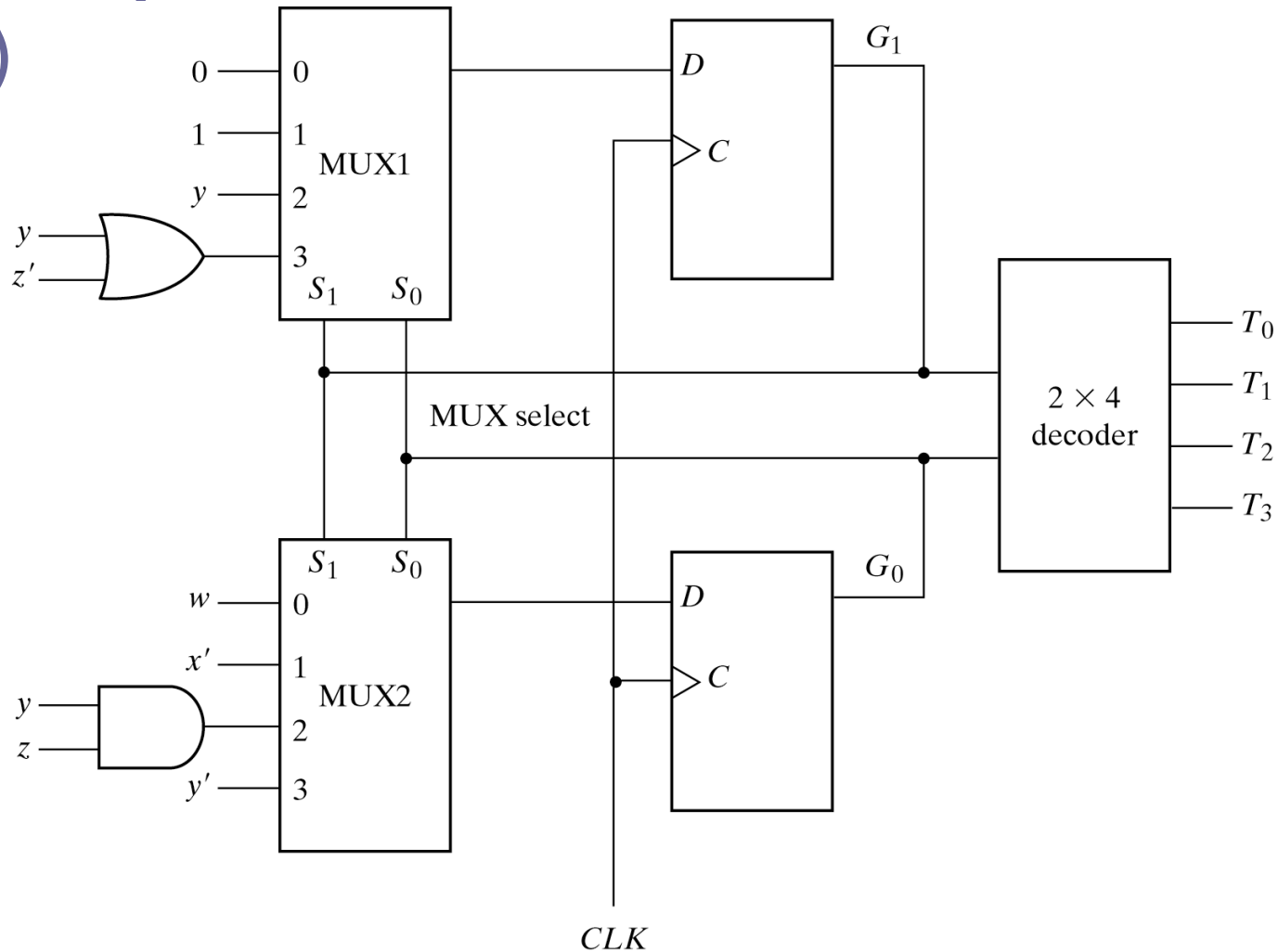Example of ASM Chart with Four Control Inputs

Example (2/4)

Control Implementation with Multiplexers

Example
(3/4) – MUX Input Conditions

Present State		Next State		Input Conditions	Inputs	
G_1	G_0	G_1	G_0		MUX1	MUX2
0	0	0	0	w'		
0	0	0	1	w	0	w
0	1	1	0	x		
0	1	1	1	x'	1	x'
1	0	0	0	y'		
1	0	1	0	yz'	yz' + yz = y	yz
1	0	1	1	yz		
1	1	0	1	y'z		
1	1	1	0	y	y + y'z' = y + z'	y'z + y'z' = y'
1	1	1	1	y'z'		

Example (4/4)

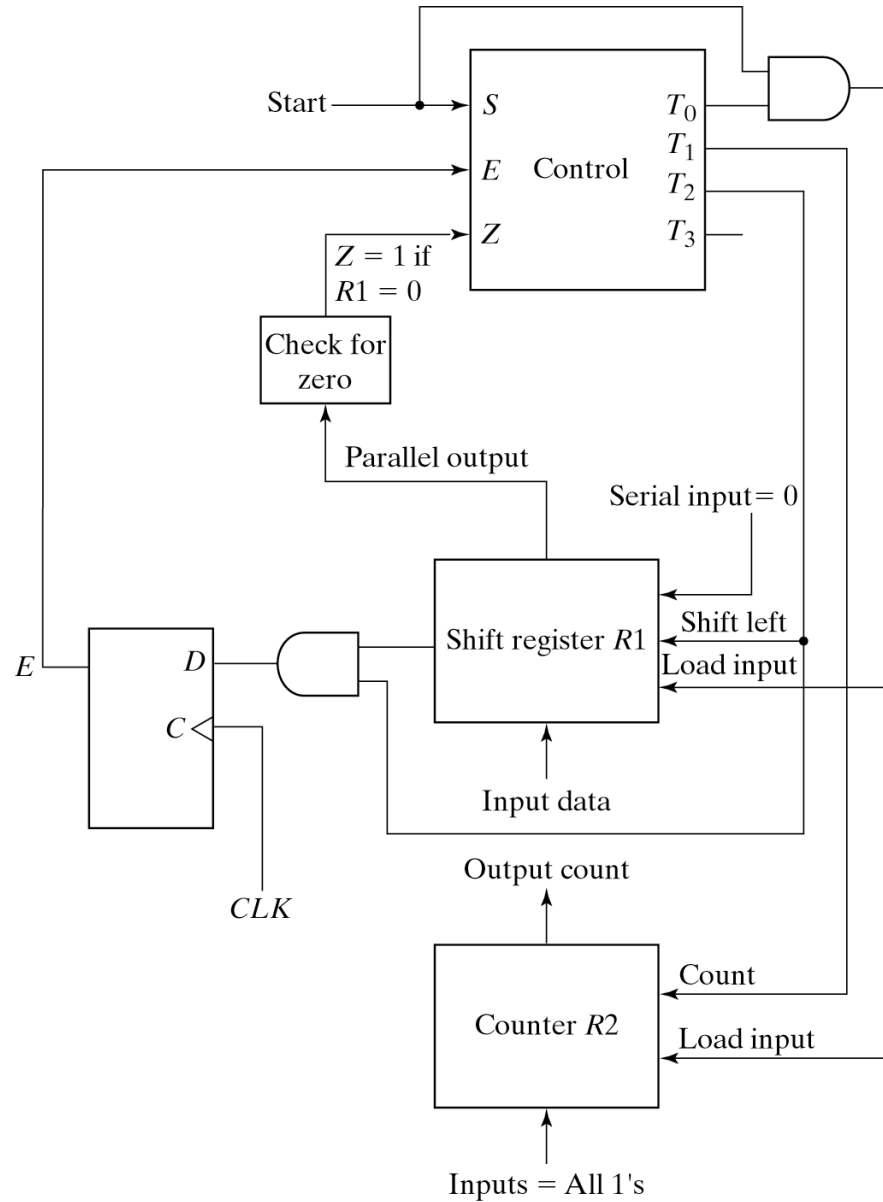Control Implementation with Multiplexers
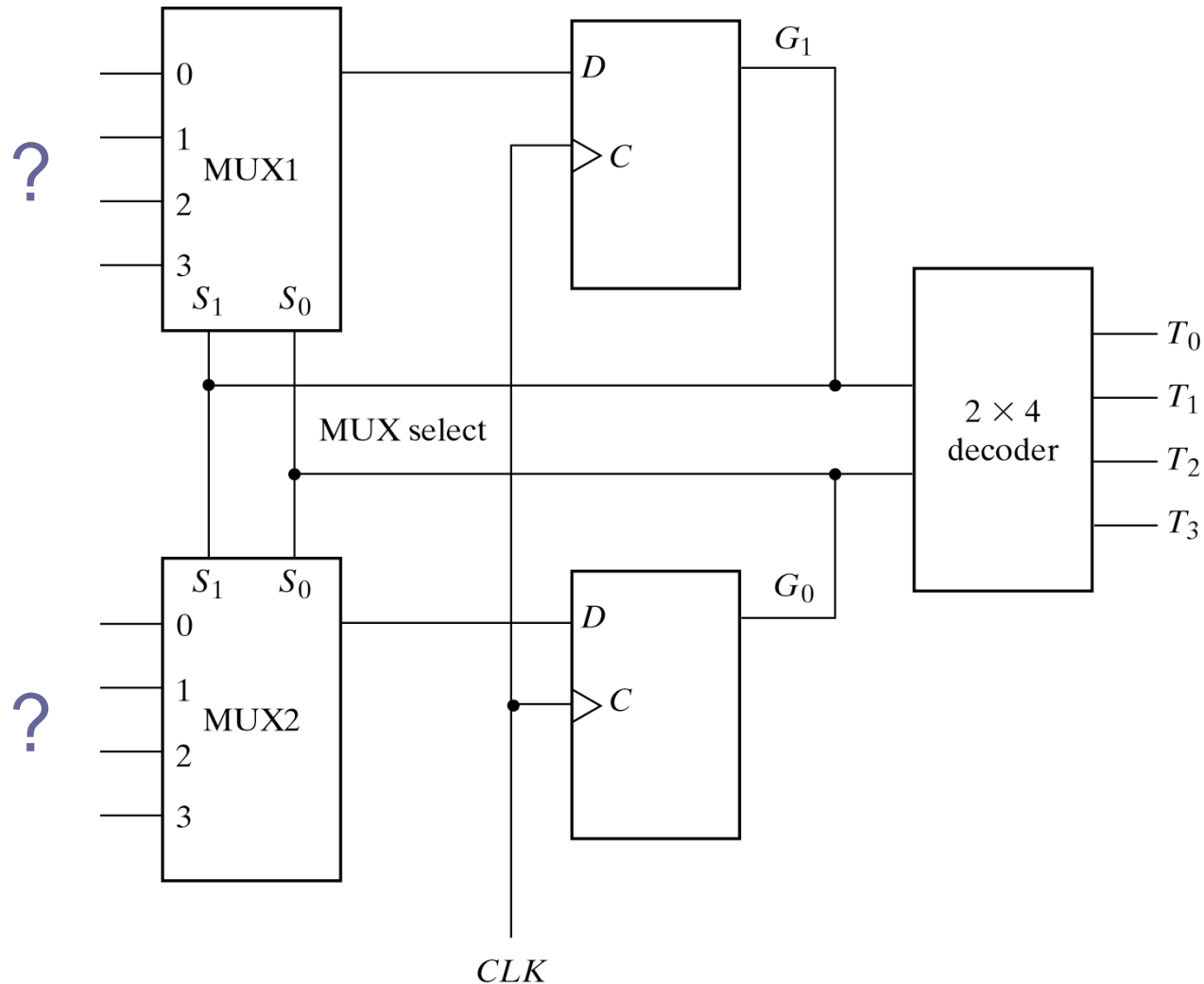
Example – Count the number of 1's
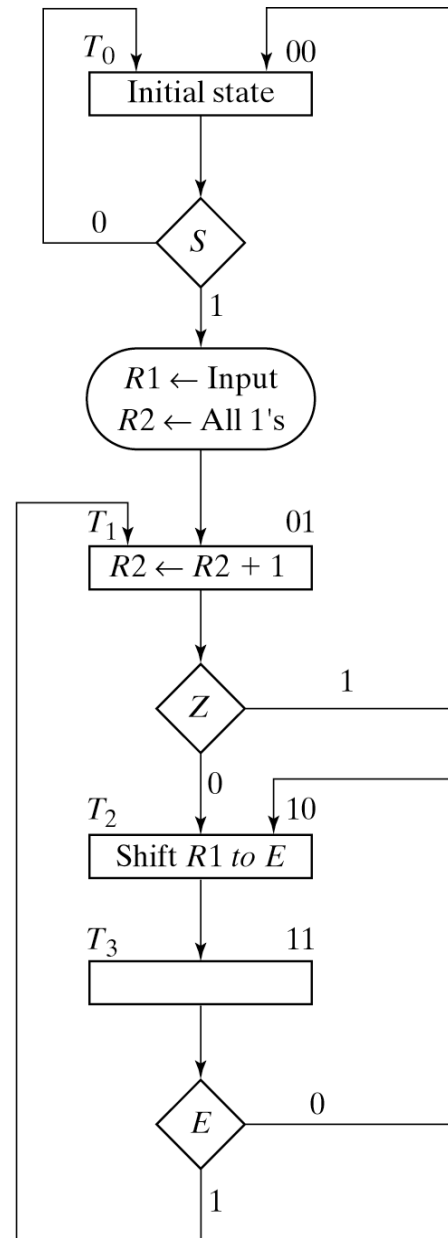
ASM Chart for Count-of-Ones Circuit

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Datapath

Block Diagram for Count-of-Ones

Control Implementation

MUX Input Conditions

Present State		Next State		Input Conditions	Inputs	
G_1	G_0	G_1	G_0		MUX1	MUX2
0	0	0	0	S'		
0	0	0	1	S	0	S
0	1	0	0	Z		
0	1	1	0	Z'	Z'	0
1	0	1	1	None	1	1
1	1	1	0	E'		
1	1	0	1	E	E'	E

Control Implementation

Control Implementation for Count-of-Ones Circuit
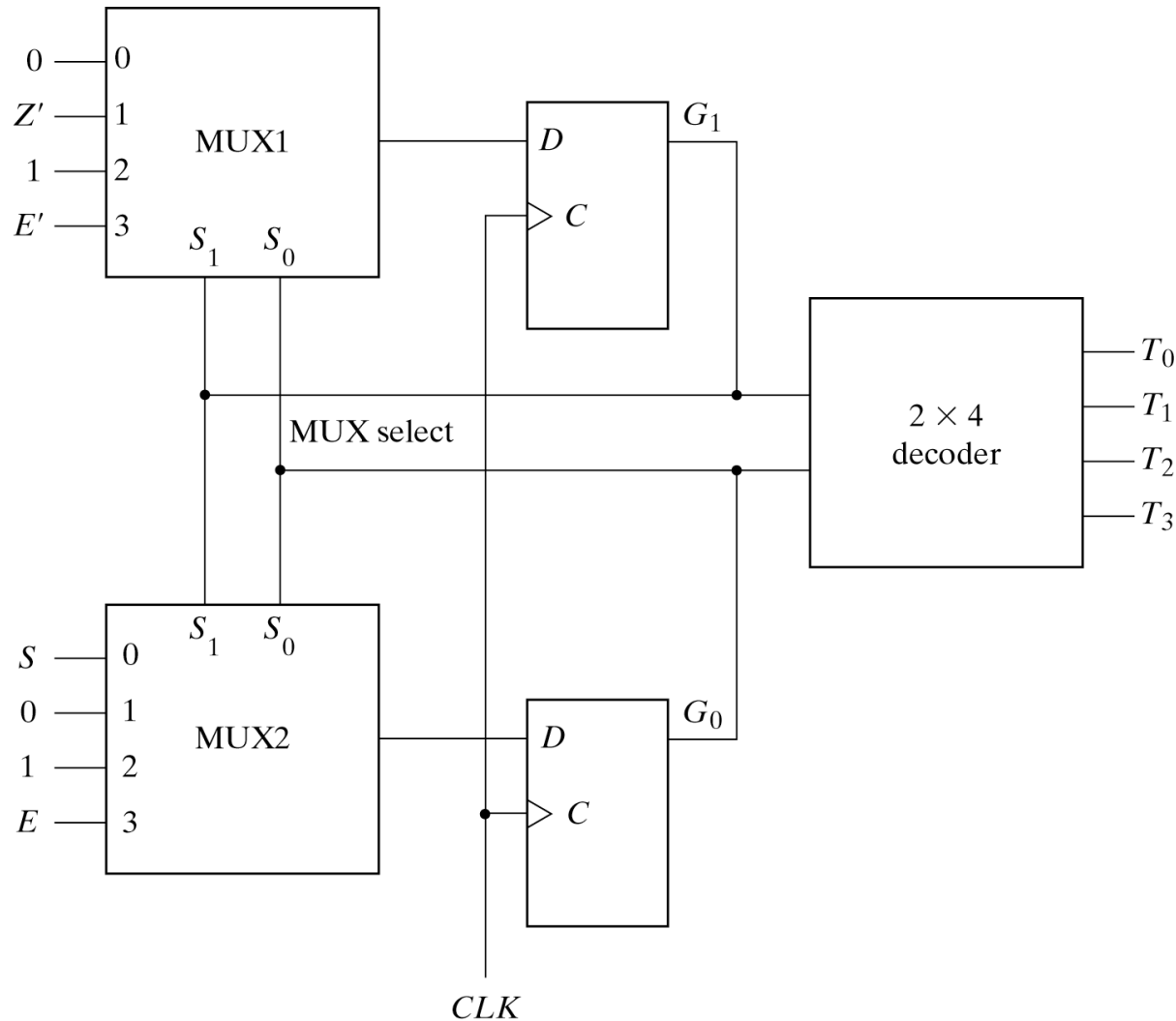
Corresponding Chapter in Textbook

- **Chapter 8** *(entire chapter)*
- **Reading Assignments**
  - Verilog HDL code (behavioral and structural) for the design example(s) given in the lecture (try to implement it yourself)
  - Design Example – Binary Multiplier
  - Design using one-hot assignment

References

- Digital Design, M. Morris, Mano