EECS 3201: Digital Logic Design Lecture 7
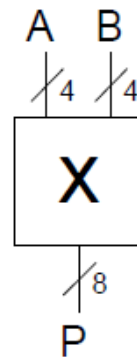
Ihab Amer, PhD, SMIEEE, P.Eng.

2x2 binary multiplier
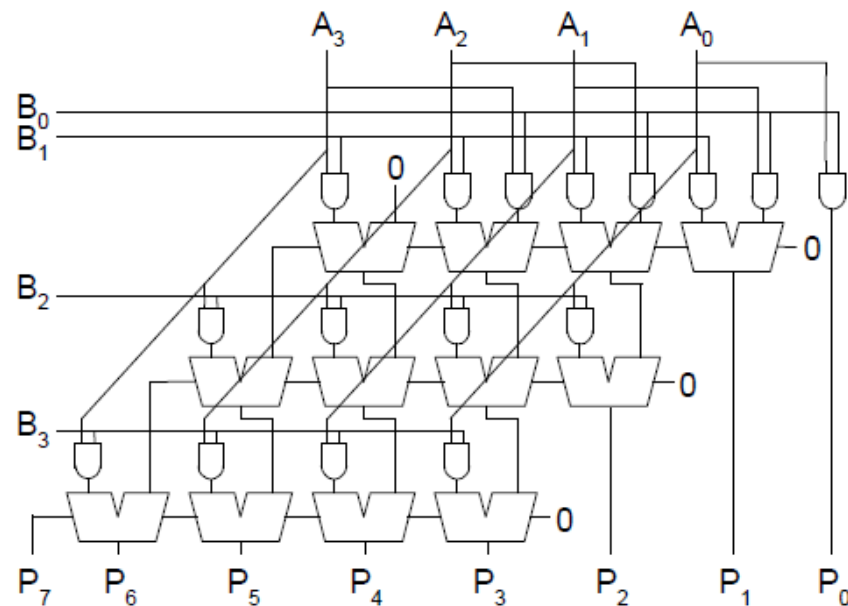

2

4x4 Array Multiplier

$$
\begin{array}{ccccc}
 & A_3 & A_2 & A_1 & A_0 \\
\times & B_3 & B_2 & B_1 & B_0 \\
\hline
 & A_3B_0 & A_2B_0 & A_1B_0 & A_0B_0 \\
 A_3B_1 & A_2B_1 & A_1B_1 & A_0B_1 & \\
 A_3B_2 & A_2B_2 & A_1B_2 & A_0B_2 & \\
+ \quad A_3B_3 & A_2B_3 & A_1B_3 & A_0B_3 & \\
\hline
P_7 \quad P_6 & P_5 & P_4 & P_3 \quad P_2 & P_1 \quad P_0 \\
\end{array}
$$

Multiplexer (MUX)

- Selects between one of N inputs to connect to output
- $\log_2 N$-bit select input – control input
- Example:

2:1 Mux
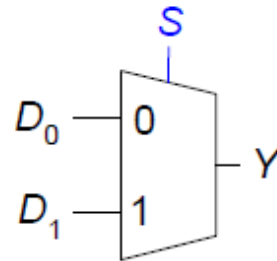
S	D_1	D_0	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

S	Y
0	D_0
1	D_1

4

MUX Implementations

- **Logic gates**
  - sum-of-products form
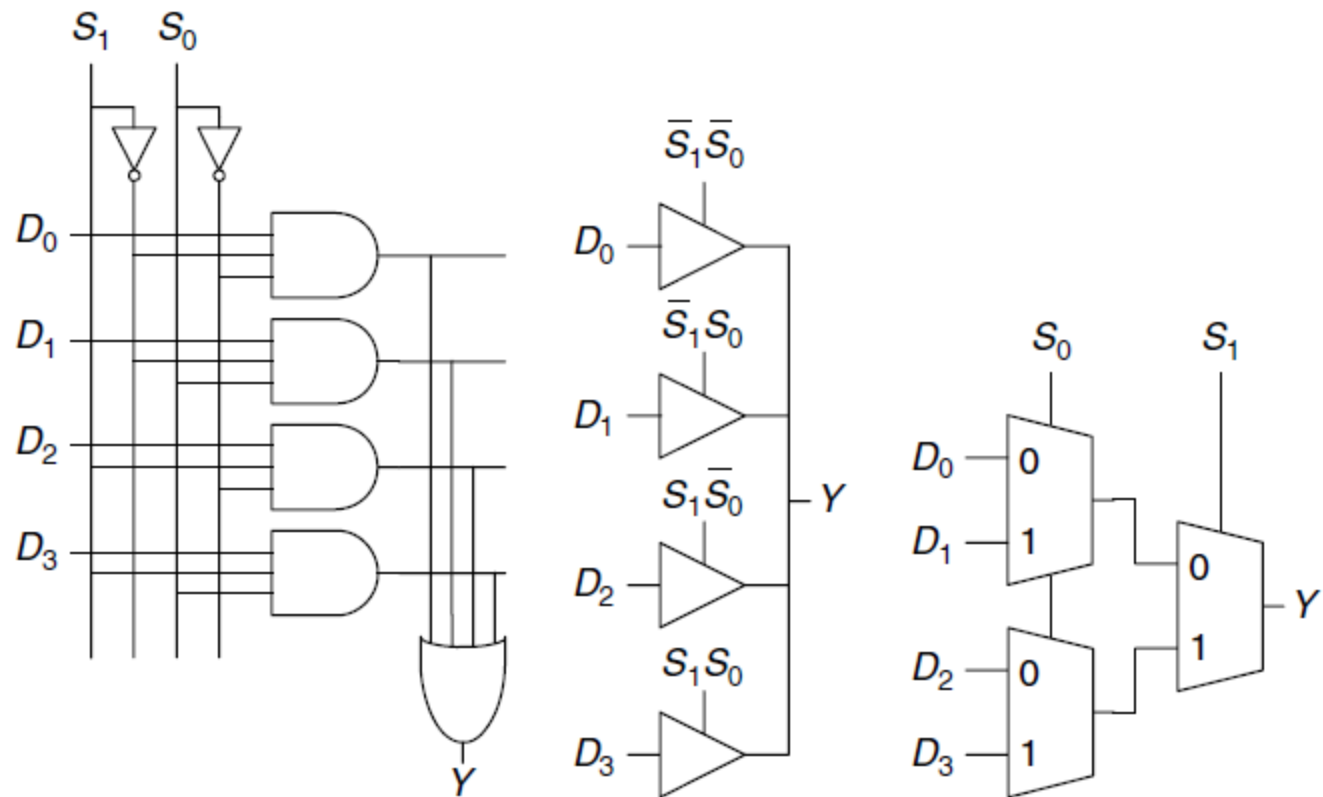
$$Y = D_0\overline{S} + D_1 S$$
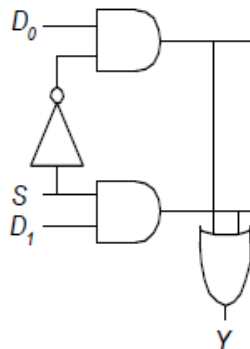
- **Tristates**
  - for an N-input mux, use N tristates
  - turn on exactly one to select an appropriate input
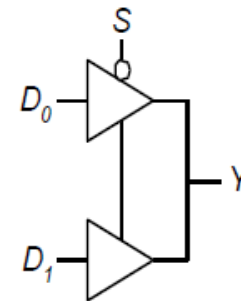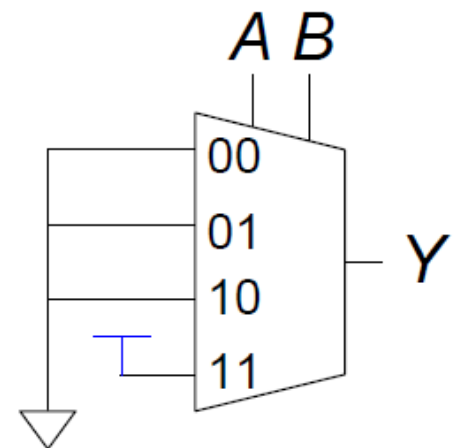
Wider MUXes

- Any of a number of options
  - depends on technology

Logic with MUXes

- Using the mux as a look-up-table
  - N-input logic gate can be represented with a 2^N input mux

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

$$Y = AB$$

A B

```
      ┌──────┐
   ───┤00    │
   ───┤01    ├─── Y
   ───┤10    │
   ───┤11    │
      └──────┘
```

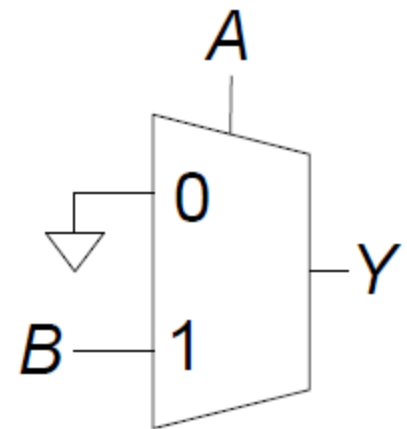# Reducing the MUX Size

- Actually…
  - N-input logic gate can be represented with a 2^{N-1} mux
  - Provide one of the literals as an input

$$Y = AB$$

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

A	Y
0	0
1	B

Mux this!

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

$$Y = A\overline{B} + \overline{B}\,\overline{C} + \overline{A}BC$$

Decoders

- N inputs, 2^N outputs
- One-hot outputs: only one output HIGH at once
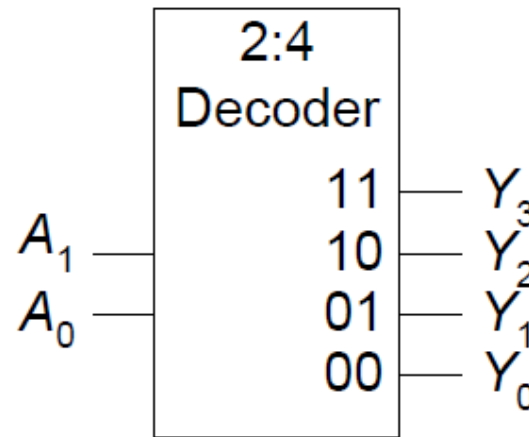
A_1	A_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

Decoder Implementation

- 2^N N-input AND gates

A_1 A_0

A_1	A_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

Y_3

Y_2

Y_1
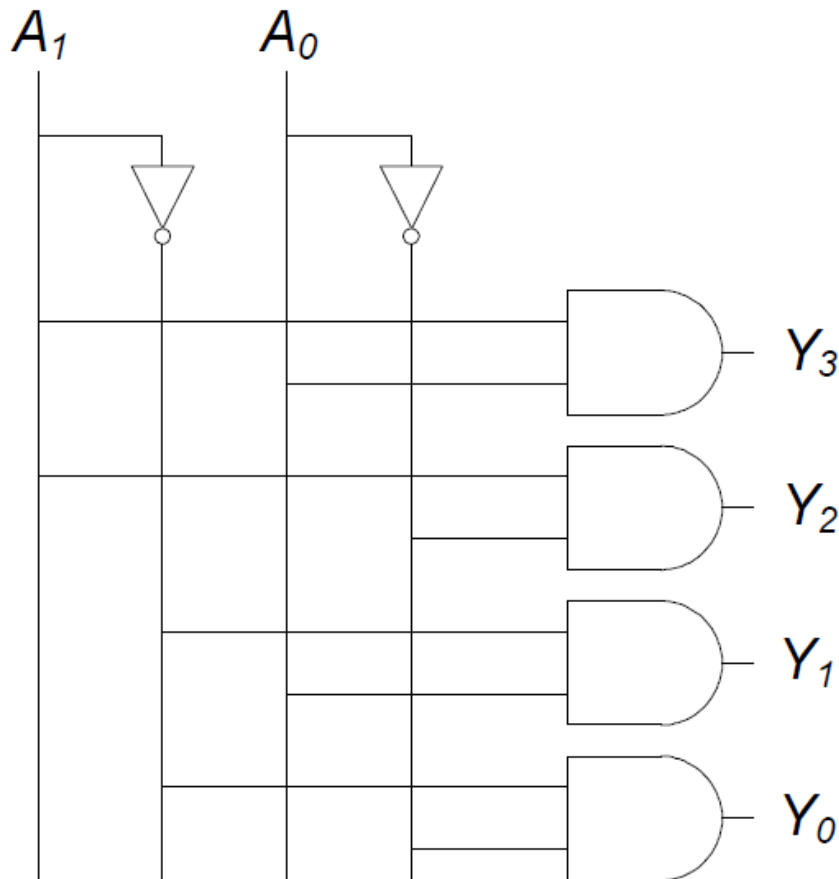
Y_0

4x16 Decoder out of 3x8 ones
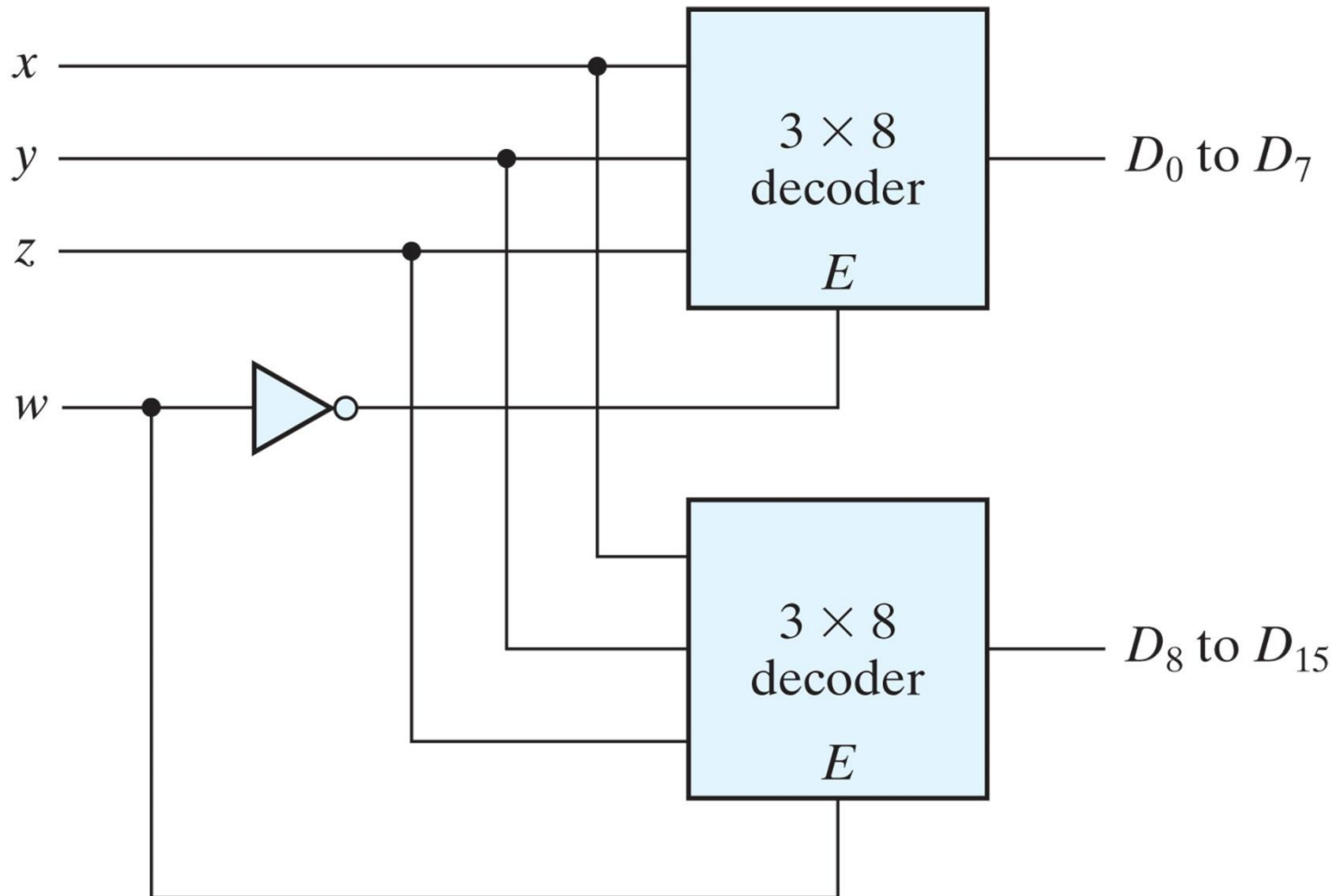
Logic Using Decoders

- OR minterms

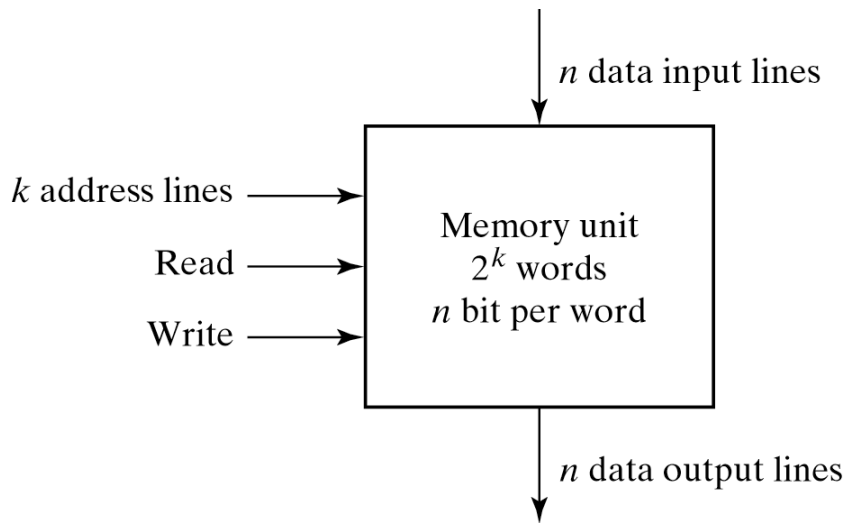$$Y = AB + \overline{A}\,\overline{B}$$
$$= \overline{A \oplus B}$$
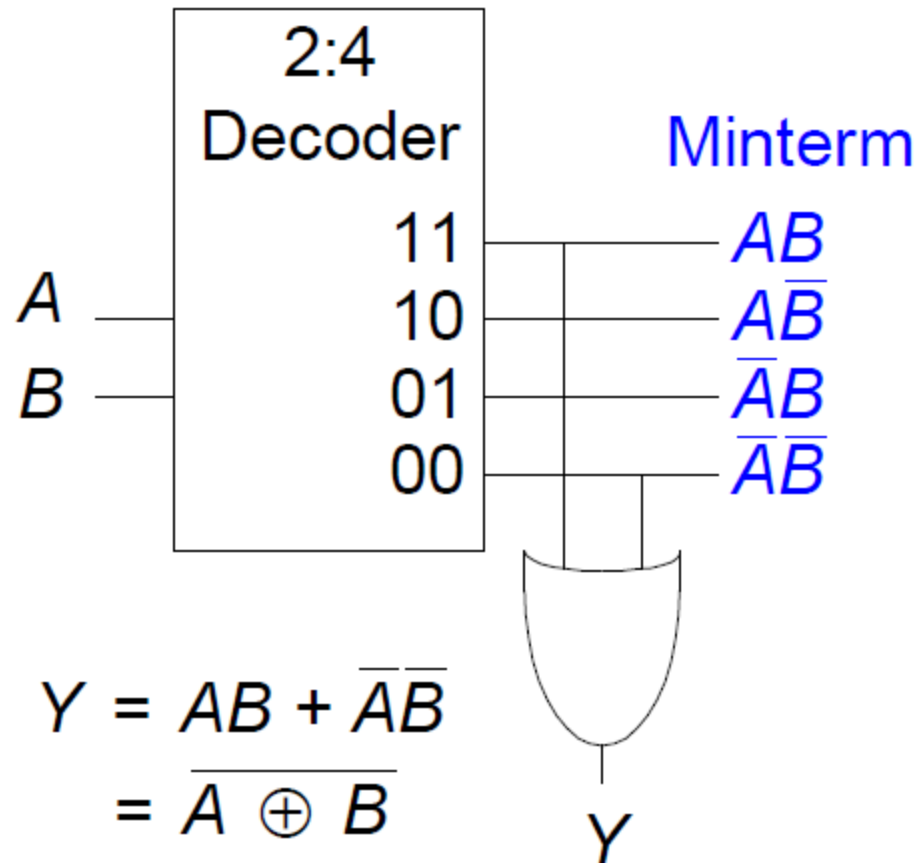
Memory

- Most real-world digital systems do contain one or more memory units

- A memory unit is a device to which binary information is transferred for storage and from which information is retrieved when needed for processing

Random-Access Memory (RAM)

Block Diagram of a Memory Unit

- n data input lines
- k address lines
- Read
- Write
- Memory unit 2^k words n bit per word
- n data output lines

Memory address		Memory contest
Binary	decimal	
0000000000	0	1011010101011101
0000000001	1	1010101110001001
0000000010	2	0000110101000110
⋮	⋮	⋮
1111111101	1021	1001110100010100
1111111110	1022	0000110100011110
1111111111	1023	1101111000100101

Content of a 1024 × 16 Memory

Memory Addressing

In order to read or write to a specific memory location, a binary code is placed on the *address bus*. Internal decoders decode the address to determine the specific location. Data is then moved to or from the *data bus*.

The address bus is a group of conductors with a common function. Its size determines the number of locations that can be accessed. A 32 bit address bus can access 2^{32} locations, which is approximately 4G.

Read   Write

Row address decoder

Address bus
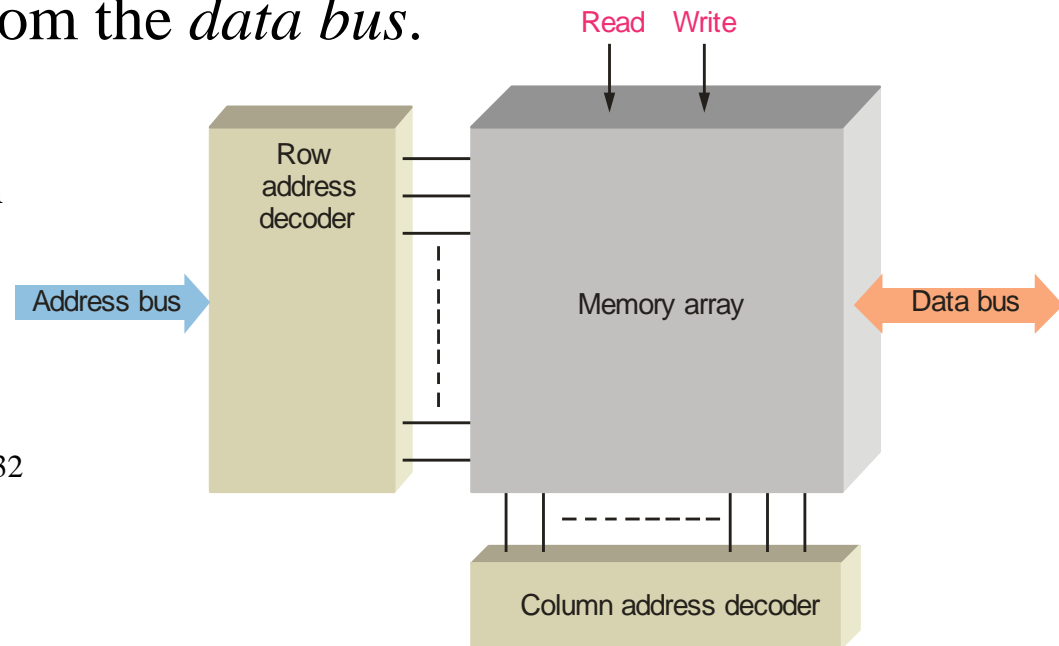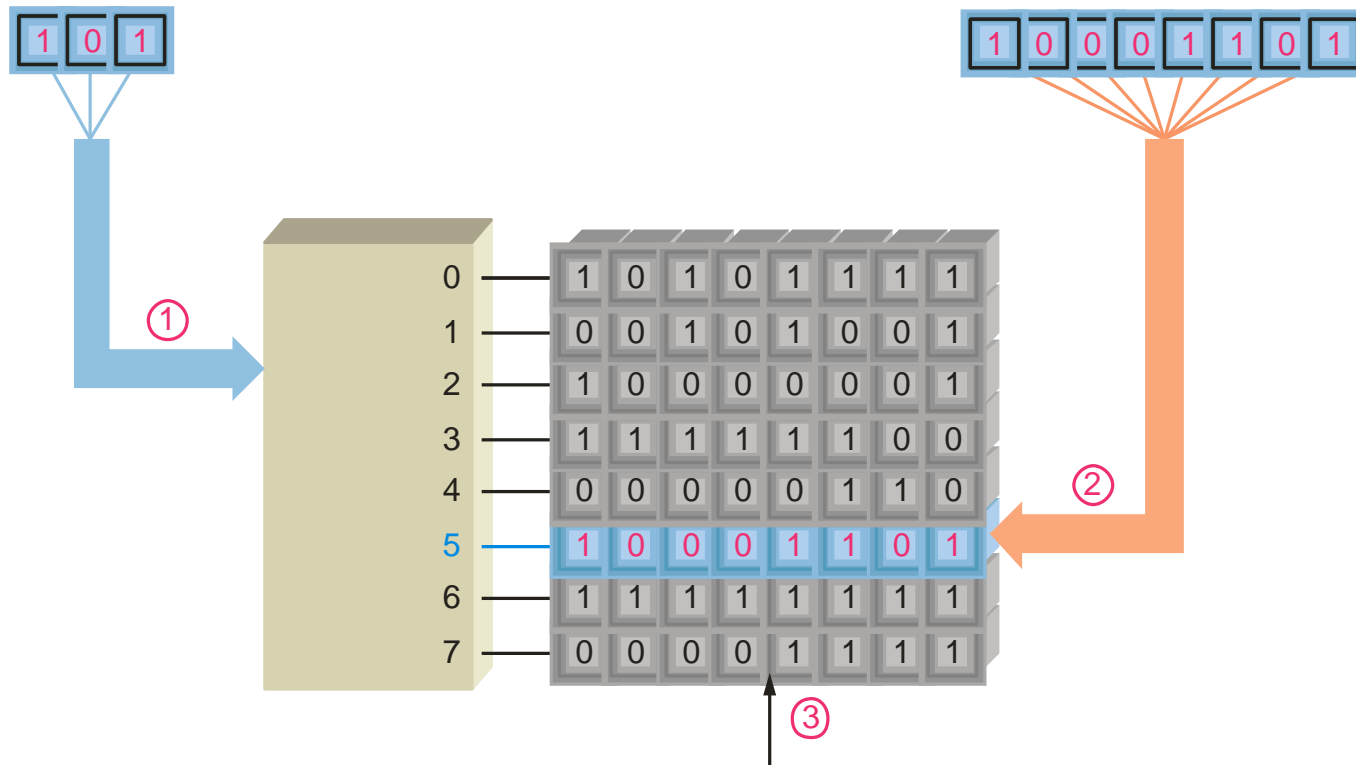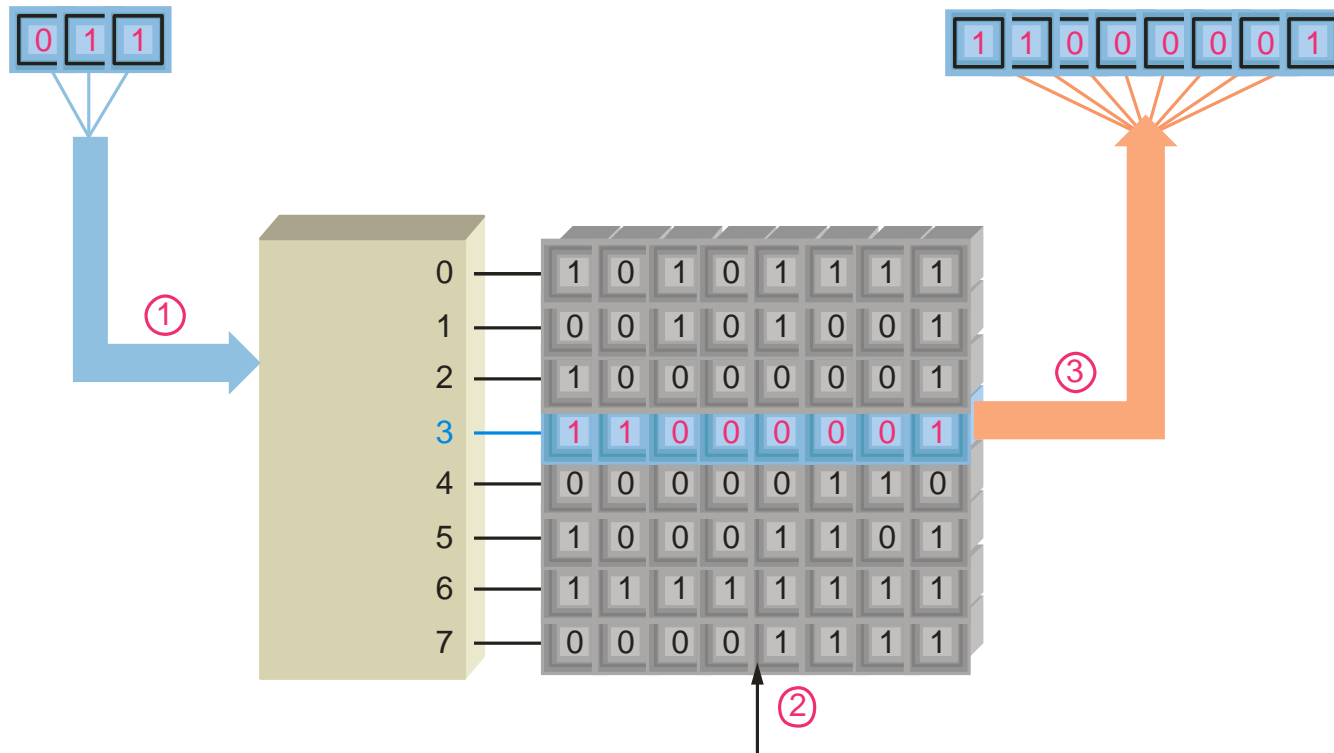
Memory array

Data bus

Column address decoder
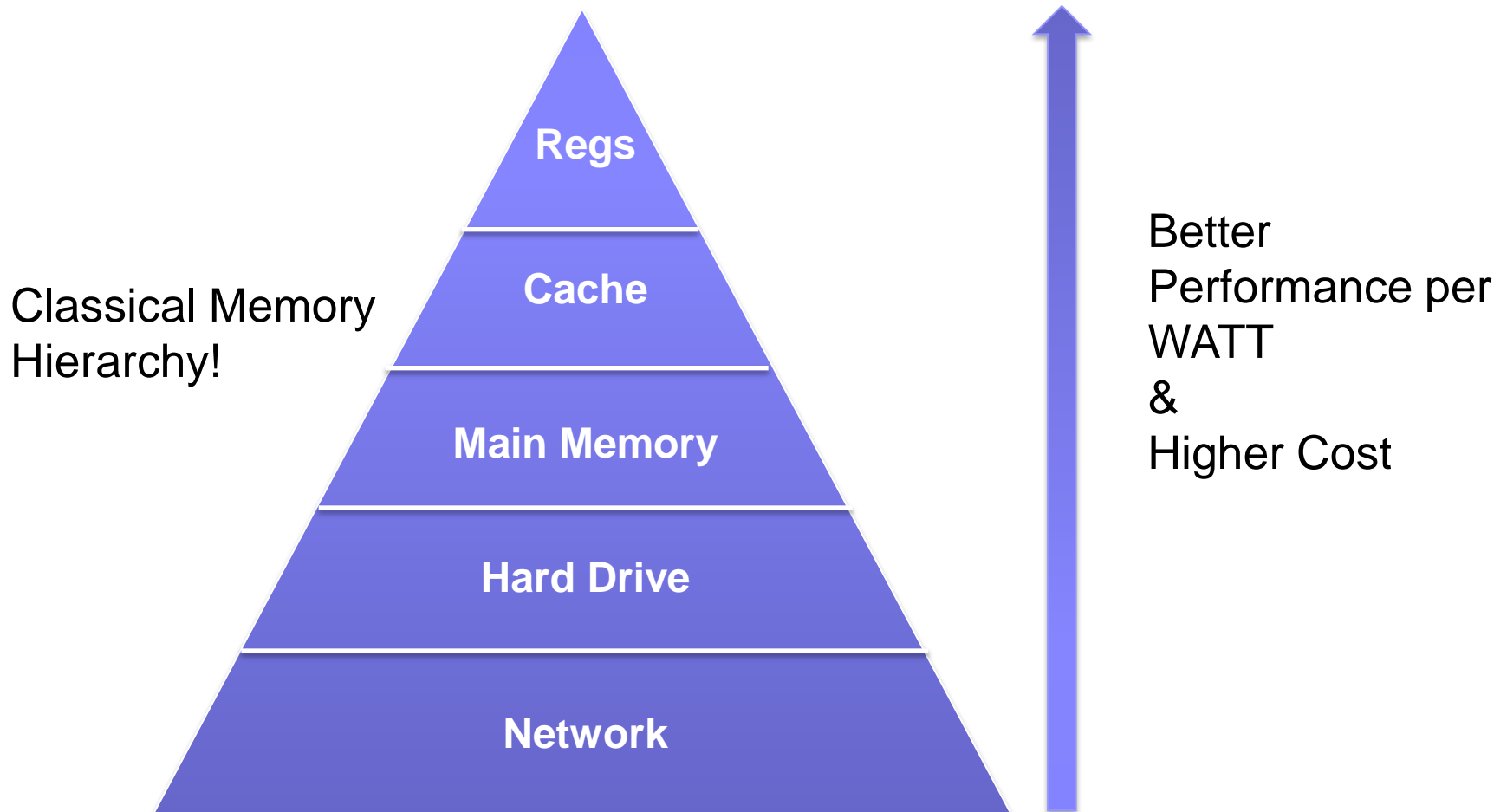
Illustration of the *Write* Operation

1. The address is placed on the address bus.
2. Data is placed on the data bus.
3. A write command is issued.

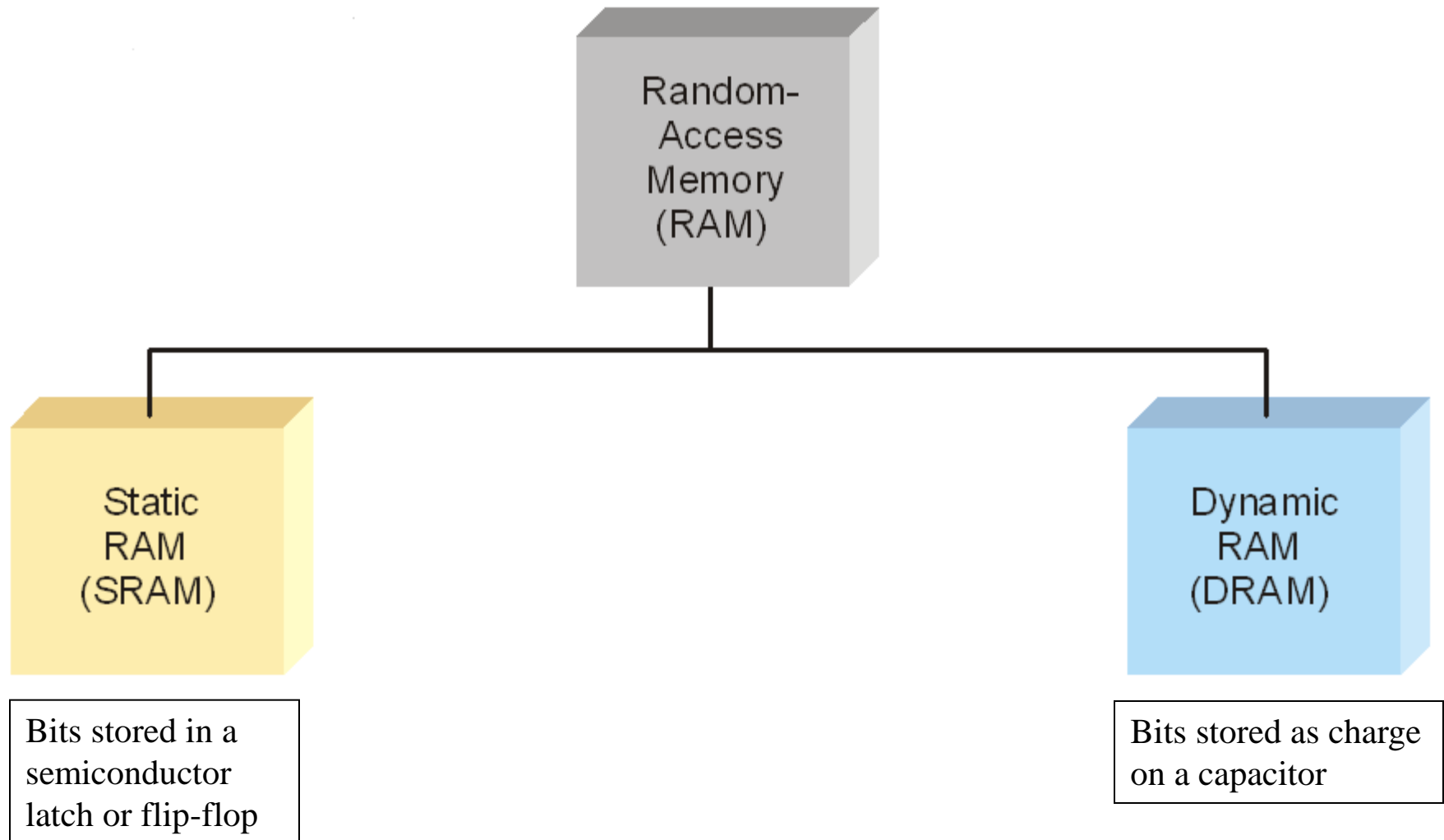# Illustration of the *Read* Operation

1. The address is placed on the address bus
2. A read command is issued
3. A copy of the data is placed in the data bus and shifted into the data register

Memory Speed Vs Cost

Classical Memory Hierarchy!

Regs

Cache

Main Memory

Hard Drive

Network

Better
Performance per
WATT
&
Higher Cost

Major RAM Types

Random-Access Memory (RAM)

Static RAM (SRAM)

Bits stored in a semiconductor latch or flip-flop

Dynamic RAM (DRAM)

Bits stored as charge on a capacitor

Static RAM (SRAM)

SRAM uses semiconductor latch memory cells. The cells are organized into an array of rows and columns
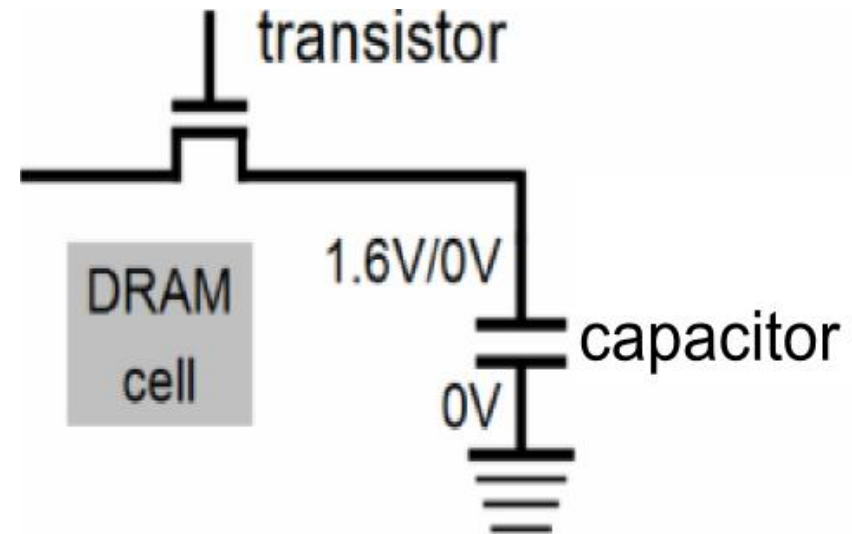
SRAM is faster than DRAM but is more complex, takes up more space, and is more expensive. SRAMs are available in many configurations – a typical large SRAM is organized as 512 k X 8 bits
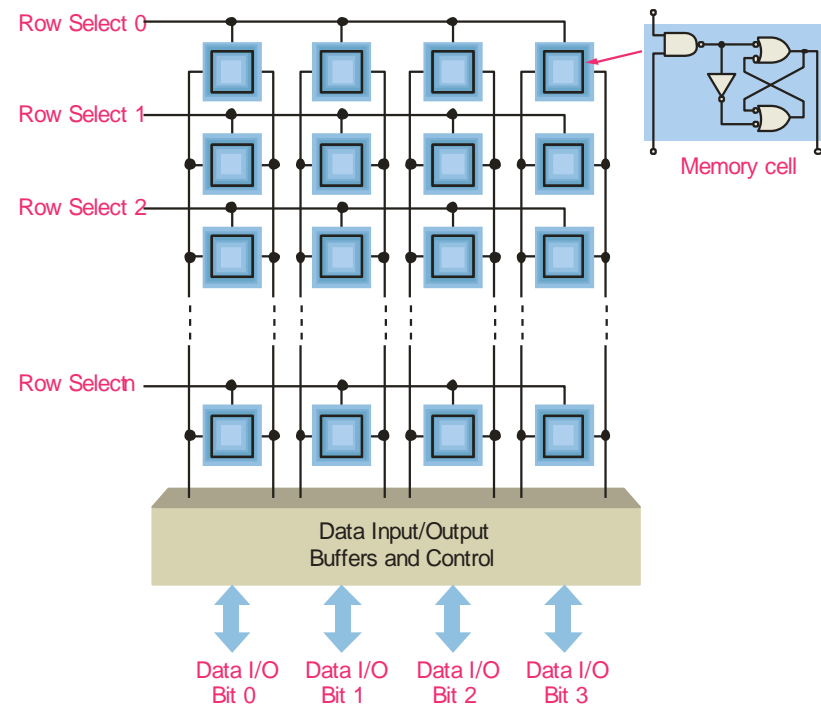
Dynamic RAM (DRAM)

Dynamic RAMs (DRAMs) store data bits as a charge on a capacitor.

DRAMs are simple and cost effective, but require refresh circuitry to prevent losing data
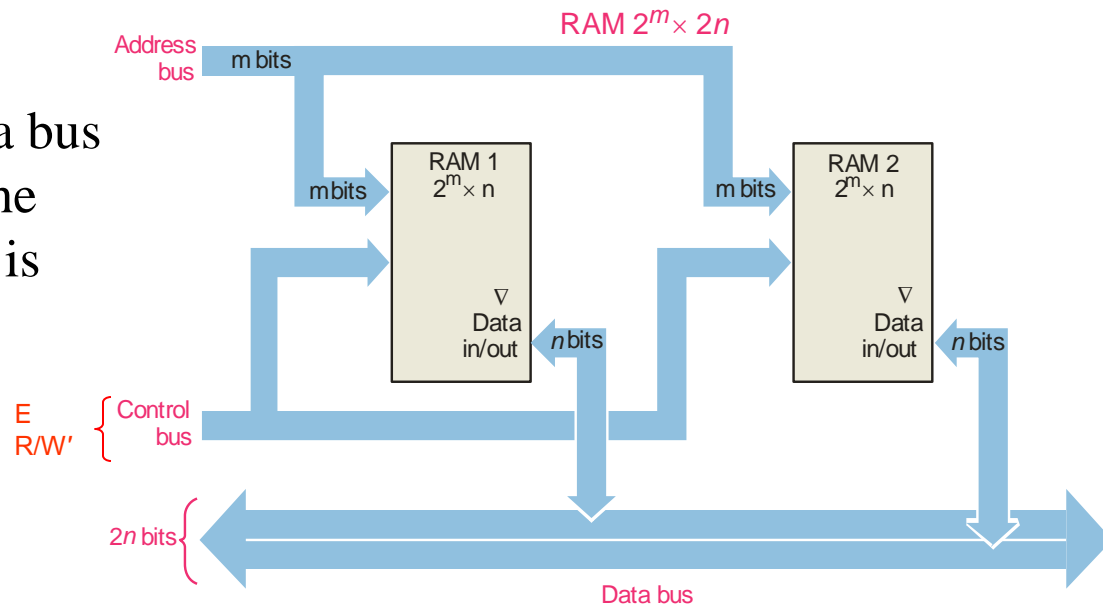
Memory Expansion (1/2)

Memory can be expanded in either word size or word capacity or both.
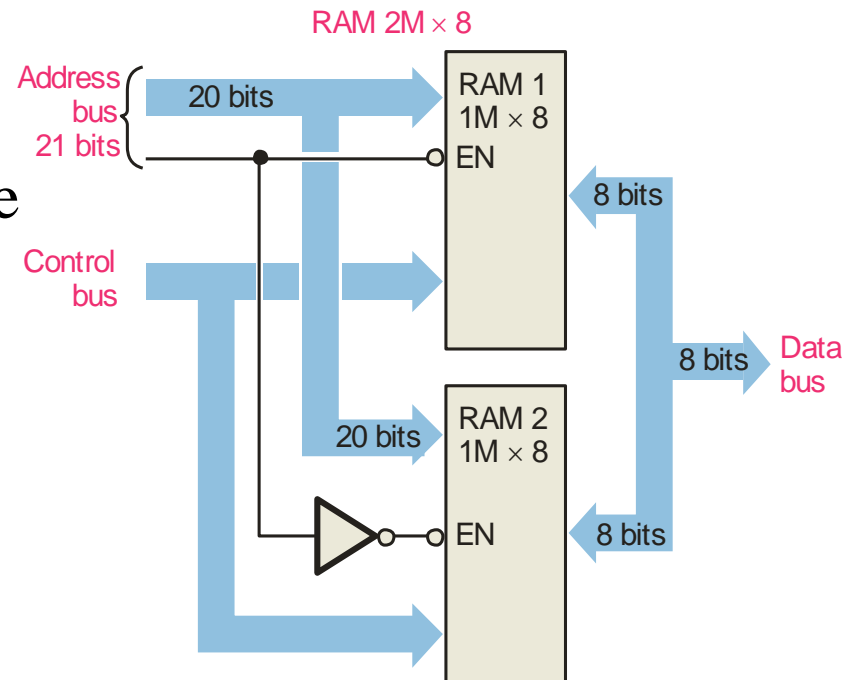
To expand word size:

Notice that the data bus size is larger, but the number of address is the same.

Memory Expansion (2/2)

To expand word capacity, you need to add an address line as shown in this example

Notice that the data bus size does not change

RAM 2M × 8

Address bus — 20 bits → RAM 1 1M × 8 EN
21 bits

8 bits

Control bus

Data bus
8 bits

20 bits → RAM 2 1M × 8

EN
8 bits

SIMMs and DIMMs

SIMMs (single in-line memory modules) and DIMMs (dual in-line memory modules) are plug-in circuit boards containing the ICs and I/O brought out on edge connectors. SIMMs have a 32-bit data path with I/O on only one side whereas DIMMs have a 64-bit data path with I/O on both sides of the board.

SIMM or DIMM

Socket on system board
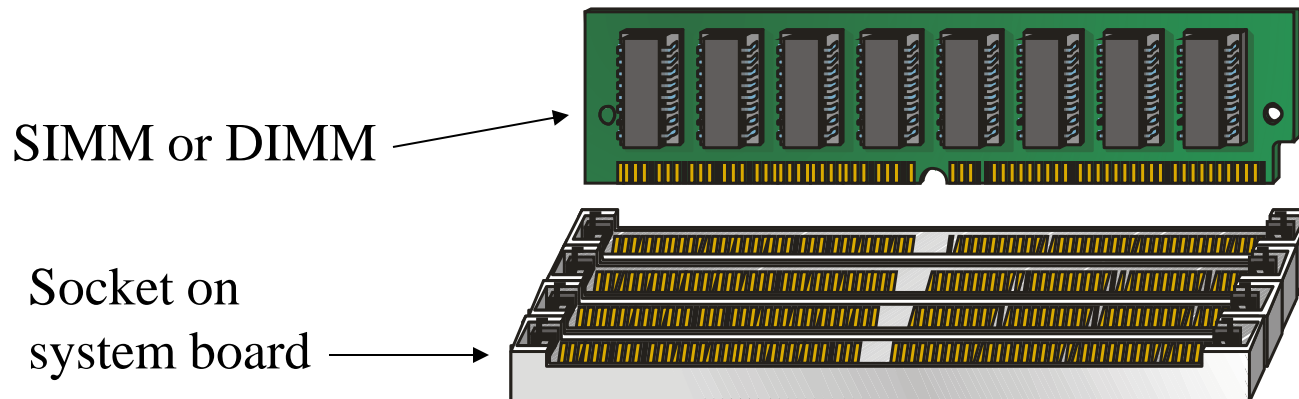
References

- Lecture Notes of Dr. Sebastian Magierowski – Fall 2013

- "Digital Design (3rd and 4th Editions)", Morris Mano , Prentice Hall, (2002/2007)

- "Digital Fundamentals (10th Edition)", Thomas L. Floyd, Prentice Hall, 2010

- http://ece.gmu.edu/coursewebpages/ECE/ECE448/S10/