3.3

Pipeline 1	Pipeline 2
LD F2, 0(Rx)	-----
~	
~	
~	
~	
Divd F8, F2, F0	MuL F7, F6, F2
LD F4, 0(Ry)	
for LD { ~	
~	
~	
~ }	
ADD F4, F0, F4	
ADDD F10, F8, F2	ADDI Rx, Rx, #8
ADDI Ry, Ry, #8	SD F4, 0(Ry)
SUB R20, R4, Rx	BNZ
~~	

22 cycles.

3.4

* If N causes an exception & N+1 finished?
* Interrupts as above * have same Rd
LD Finishes before Div & MUL

3.5 one way

```
LD F2,          LD F4,
 ~               ~
 ~               ~
 ~               ~
 ~               ~
DIV F8,F2,F0    ADDD F4,F0,F4
MUL F2,F6,F2     ~
                 SD F4,...
```

wait 11 cycles

```
ADDD F10,F8,F2
 ~
```