

3.3

Pipeline 1

LD F2,0(Rx)

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Divd F8, F2, F0  
LD F4, 0(Ry)

Pipeline 2

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MUL F2, F6, F2

for LD {

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ADD F4, F0, F4

ADDD F10, F8, F2

ADDI Ry, Ry, #8

SUB RP0, RP4/RX

ADDI RX, RX, #8

SD F4, 0(Ry)

BNZ

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22 cycles.

3.4

\* If N causes an exception & N+1 finished?

\* Interrupts as above \* have same Rd

LD Finishes before DIV & MUL



Managing the National Design Network

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3.5 one way

LD F2,

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DIU F8, F2, F0  
MUL F2, F6, F2

} wait 11 cycles

LD F4,

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ADD F4, F0, F4

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SD F4, ...

ADD F10, F8, F2

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