

CSE 2021 Computer Organization

Appendix C

Activities

Activity 1

Derive SOP and POS expressions for the following TT.

A	B	Carry
0	0	0
0	1	0
1	0	0
1	1	1

Activity 1

Derive SOP and POS expressions for the following TT.

A	B	Carry	Minterms	Maxterms
0	0	0	A'B'	A+B
0	1	0	A'B	A+B'
1	0	0	AB'	A'+B
1	1	1	AB	A'+B'

SOP: Carry=AB

POS: Carry=(A+B)(A+B')(A'+B)

Activity 2

Proofs of some Identities:

$$12b: \quad A + \overline{A}B = A + B$$

$$13a: \quad AB + \overline{A}C + BC = AB + \overline{A}C$$

Activity 2

Proofs of some Identities:

$$A + \overline{A}B = A + B$$

$$\begin{aligned} 12b: \quad A + \overline{A}B &= A + AB + \overline{A}B \quad (A + AB = A(B + 1) = A) \quad (\text{Using 11}) \\ &= A + B \end{aligned}$$

$$AB + \overline{A}C + BC = AB + \overline{A}C$$

$$\begin{aligned} 13a: \quad &= AB + \overline{A}C + (A + \overline{A})BC \\ &= AB + \overline{A}C + ABC + \overline{A}BC \\ &= AB(C + 1) + \overline{A}C(B + 1) \\ &= AB + \overline{A}C \end{aligned}$$

Activity 3

- Find an MSOP for

$$F = V\overline{W}XY + VWYZ + V\overline{X}YZ$$

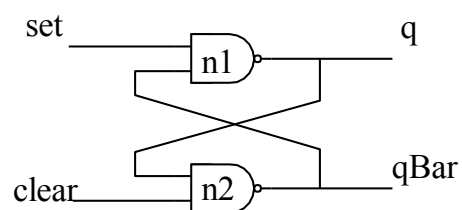
Activity 3

- Find an MSOP for

$$\begin{aligned}
 F &= V\overline{W}XY + VWYZ + V\overline{X}YZ \\
 &= VY(\overline{W}X + WZ + \overline{X}Z) \\
 &= VY(\overline{W}X + Z(W + \overline{X})) \quad [W + \overline{X} = \overline{\overline{W}X}] \\
 &= VY(\overline{W}X + Z\overline{\overline{W}X}) \quad [A + \overline{A}B = A + B] \\
 &= VY(\overline{W}X + Z) \\
 &= VY\overline{W}X + VYZ
 \end{aligned}$$

Activity 4

Given the circuit below, develop a Verilog module for the circuit



Activity 4

```
Module simple_latch (q, qBar, set, clear);  
  input set, clear;  
  output q, qBar;  
  nand #2 n1(q,qBar,set);  
  nand #2 n2(qBar,q,clear);  
endmodule
```

