1.5

a. performance of P1 (instructions/sec) $= 3 \times 10^9/1.5 = 2 \times 10^9$
performance of P2 (instructions/sec) $= 2.5 \times 10^9/1.0 = 2.5 \times 10^9$
performance of P3 (instructions/sec) $= 4 \times 10^9/2.2 = 1.8 \times 10^9$

1.6

a. Class A: 10^5 instr. Class B: 2×10^5 instr. Class C: 5×10^5 instr. Class D: 2×10^5 instr.

Time = No. instr. × CPI/clock rate

Total time P1 = $(10^5 + 2 \times 10^5 \times 2 + 5 \times 10^5 \times 3 + 2 \times 10^5 \times 3)/(2.5 \times 10^9) = 10.4 \times 10^{-4}$ s

Total time P2 = $(10^5 \times 2 + 2 \times 10^5 \times 2 + 5 \times 10^5 \times 2 + 2 \times 10^5 \times 2)/(3 \times 10^9) = 6.66 \times 10^{-4}$ s

CPI(P1) = $10.4 \times 10^{-4} \times 2.5 \times 10^9/10^6 = 2.6$

CPI(P2) = $6.66 \times 10^{-4} \times 3 \times 10^9/10^6 = 2.0$

b. clock cycles(P1) = $10^5 \times 1 + 2 \times 10^5 \times 2 + 5 \times 10^5 \times 3 + 2 \times 10^5 \times 3 = 26 \times 10^5$

clock cycles(P2) = $10^5 \times 2 + 2 \times 10^5 \times 2 + 5 \times 10^5 \times 2 + 2 \times 10^5 \times 2 = 20 \times 10^5$

1.7

a. CPI = $T_{exec} \times$ f/No. instr.

Compiler A CPI = 1.1

Compiler B CPI = 1.25

b. f_B/f_A = (No. instr.(B) × CPI(B))/(No. instr.(A) × CPI(A)) = 1.37

c. $T_A/T_{new} = 1.67$

$T_B/T_{new} = 2.27$

1.8

1.8.1 $C = 2 \times DP/(V^{2*}F)$

Pentium 4: $C = 3.2E{-}8F$

Core i5 Ivy Bridge: $C = 2.9E{-}8F$

1.8.2 Pentium 4: $10/100 = 10\%$

Core i5 Ivy Bridge: $30/70 = 42.9\%$

1.10

1.10.1 die area$_{15cm}$ = wafer area/dies per wafer = pi*7.5^2 / 84 = 2.10 cm^2

yield$_{15cm}$ = 1/(1+(0.020*2.10/2))^2 = 0.9593

die area$_{20cm}$ = wafer area/dies per wafer = pi*10^2/100 = 3.14 cm^2

yield$_{20cm}$ = 1/(1+(0.031*3.14/2))^2 = 0.9093

1.10.2 cost/die$_{15cm}$ = 12/(84*0.9593) = 0.1489

cost/die$_{20cm}$ = 15/(100*0.9093) = 0.1650

1.11

1.11.1 CPI = clock rate × CPU time/instr. count

clock rate = 1/cycle time = 3 GHz

CPI(bzip2) = $3 \times 10^9 \times 750/(2389 \times 10^9) = 0.94$

1.11.2 SPEC ratio = ref. time/execution time

SPEC ratio(bzip2) = 9650/750 = 12.86

1.11.3. CPU time = No. instr. × CPI/clock rate

If CPI and clock rate do not change, the CPU time increase is equal to the increase in the of number of instructions, that is 10%.

1.11.4 CPU time(before) = No. instr. × CPI/clock rate

CPU time(after) = 1.1 × No. instr. × 1.05 × CPI/clock rate

CPU time(after)/CPU time(before) = 1.1 × 1.05 =1.155. Thus, CPU time is increased by 15.5%.

1.11.5 SPECratio = reference time/CPU time

SPECratio(after)/SPECratio(before) = CPU time(before)/CPU time(after) = 1/1.1555 = 0.86. The SPECratio is decreased by 14%.

1.12

1.12.1 T(P1) = $5 \times 10^9 \times 0.9 / (4 \times 10^9) = 1.125$ s

T(P2) = $10^9 \times 0.75 / (3 \times 10^9) = 0.25$ s

clock rate (P1) > clock rate(P2), performance(P1) < performance(P2)

1.12.2 T(P1) = No. instr. × CPI/clock rate

T(P1) = 2.25 3 1021 s

T(P2) = N × 0.75/(3×10^9), then N = 9×10^8

1.12.3 MIPS = Clock rate × 10^{-6}/CPI

MIPS(P1) = $4 \times 10^9 \times 10^{-6}/0.9 = 4.44 \times 10^3$

$$\text{MIPS(P2)} = 3 \times 10^9 \times 10^{-6}/0.75 = 4.0 \times 10^3$$

MIPS(P1) > MIPS(P2), performance(P1) < performance(P2) (from 11a)

1.14

1.14.1 Clock cycles = $CPI_{fp} \times$ No. FP instr. + $CPI_{int} \times$ No. INT instr. + $CPI_{l/s} \times$ No. L/S instr. + $CPI_{branch} \times$ No. branch instr.

T_{CPU} = clock cycles/clock rate = clock cycles/2×10^9

clock cycles = 512×10^6; $T_{CPU} = 0.256$ s

To have the number of clock cycles by improving the CPI of FP instructions:

$CPI_{improved\ fp} \times$ No. FP instr. + $CPI_{int} \times$ No. INT instr. + $CPI_{l/s} \times$ No. L/S instr. + $CPI_{branch} \times$ No. branch instr. = clock cycles/2

$CPI_{improved\ fp}$ = (clock cycles/2 − ($CPI_{int} \times$ No. INT instr. + $CPI_{l/s} \times$ No. L/S instr. + $CPI_{branch} \times$ No. branch instr.)) / No. FP instr.

$CPI_{improved\ fp} = (256-462)/50 < 0 ==>$ not possible

1.14.2 Using the clock cycle data from a.

To have the number of clock cycles improving the CPI of L/S instructions:

$CPI_{fp} \times$ No. FP instr. + $CPI_{int} \times$ No. INT instr. + $CPI_{improved\ l/s} \times$ No. L/S instr. + $CPI_{branch} \times$ No. branch instr. = clock cycles/2

$CPI_{improved\ l/s}$ = (clock cycles/2 − ($CPI_{fp} \times$ No. FP instr. + $CPI_{int} \times$ No. INT instr. + $CPI_{branch} \times$ No. branch instr.)) / No. L/S instr.

$CPI_{improved\ l/s} = (256-198)/80 = 0.725$

1.14.3 Clock cycles = $CPI_{fp} \times$ No. FP instr. + $CPI_{int} \times$ No. INT instr. + $CPI_{l/s} \times$ No. L/S instr. + $CPI_{branch} \times$ No. branch instr.

T_{CPU} = clock cycles/clock rate = clock cycles/2×10^9

$CPI_{int} = 0.6 \times 1 = 0.6$; $CPI_{fp} = 0.6 \times 1 = 0.6$; $CPI_{l/s} = 0.7 \times 4 = 2.8$;
$CPI_{branch} = 0.7 \times 2 = 1.4$

T_{CPU} (before improv.) = 0.256 s; T_{CPU} (after improv.)= 0.171 s