Small v_{DS}

$$i_D = \left[(\mu_n C_{ox}) \left(\frac{W}{L} \right) V_{ov} \right] v_{DS}$$

Conductance

$$g_{DS} = (\mu_n C_{ox}) \left(\frac{W}{L} \right) V_{ov}$$

$$r_{DS} = \frac{1}{(\mu_n C_{ox}) \left(\frac{W}{L} \right) V_{ov}}$$

Linear resistance

Not Small v_{DS}

- As v_{DS} increases we can not assume a constant voltage between the gate and any point along the channel.
- The voltage at one end of the channel is 0, while at the other end is v_{DS}

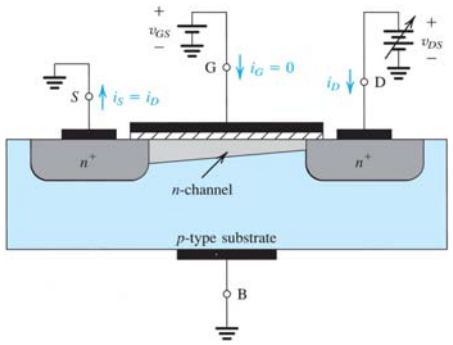


Figure 5.5 Operation of the enhancement NMOS transistor as v_{DS} is increased. The induced channel acquires a tapered shape, and its resistance increases as v_{DS} is increased. Here, v_{GS} is kept constant at a value $> V_t$; $v_{GS} = V_t + V_{OV}$.

$$i_D = \left[(\mu_n C_{ox})\left(\frac{W}{L}\right)V_{ov}\right]v_{DS}$$

$$i_D = \left[(\mu_n C_{ox})\left(\frac{W}{L}\right)\left(V_{ov} - \frac{1}{2}v_{DS}\right)\right]v_{DS}$$

$$i_D = \left[k_n'\left(\frac{W}{L}\right)\left(V_{ov} - \frac{1}{2}v_{DS}\right)\right]v_{DS}$$

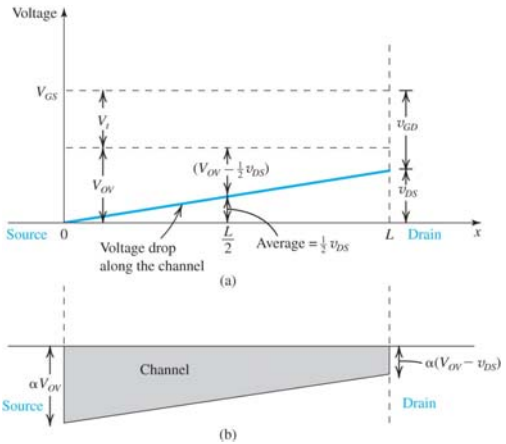


Figure 5.6 **(a)** For a MOSFET with $v_{GS} = V_t + V_{OV}$, application of v_{DS} causes the voltage drop along the channel to vary linearly, with an average value of $\frac{1}{2}v_{DS}$ at the midpoint. Since $v_{GD} > V_t$, the channel still exists at the drain end. **(b)** The channel shape corresponding to the situation in **(a)**. While the depth of the channel at the source end is still proportional to V_{OV}, that at the drain end is proportional to $(V_{OV} - v_{DS})$.

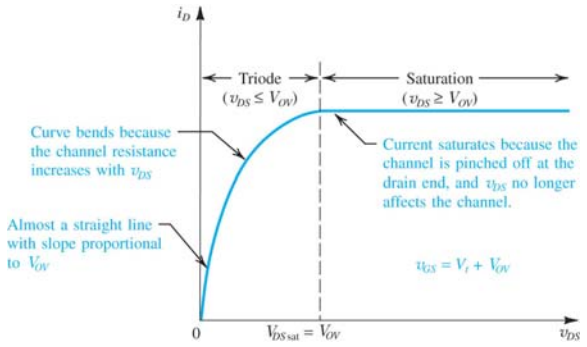


Figure 5.7 The drain current i_D versus the drain-to-source voltage v_{DS} for an enhancement-type NMOS transistor operated with $v_{GS} = V_t + V_{OV}$.

Channel Pinch-Off

- In the previous case, v_{DS} is kept small such that the $v_{GD} > V_t$
- When $v_{DS} = V_{OV}$, the channel width = 0 at the drain ➔ Pinch-Off
- Increasing v_{DS} has no effect on the channel shape and the current remains constant

$$i_D = \frac{1}{2} k_n' \left(\frac{W}{L}\right) V_{ov}^2$$

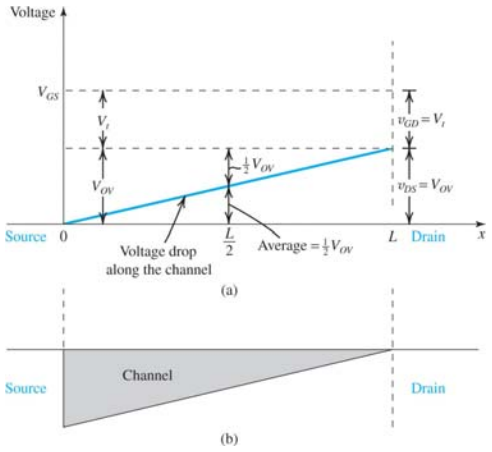


Figure 5.8 Operation of MOSFET with $v_{GS} = V_t + V_{OV}$, a s v_{DS} is increased to V_{OV}. At the drain end, v_{GD} decreases to V_t and the channel depth at the drain end reduces to zero (pinch-off). At this point, the MOSFET enters the saturation mode of operation. Further increasing v_{DS} (beyond $V_{DSsat} = V_{OV}$) has no effect on the channel shape and i_D remains constant.

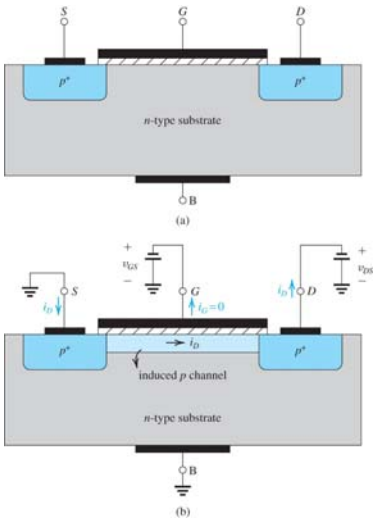


Figure 5.9 **(a)** Physical structure of the PMOS transistor. Note that it is similar to the NMOS transistor shown in Fig. 5.1(b) except that all semiconductor regions are reversed in polarity. **(b)** A negative voltage v_{GS} of magnitude greater than V_{tp} induces a p channel, and a negative v^{DS} causes a current i^D to flow from source to drain.

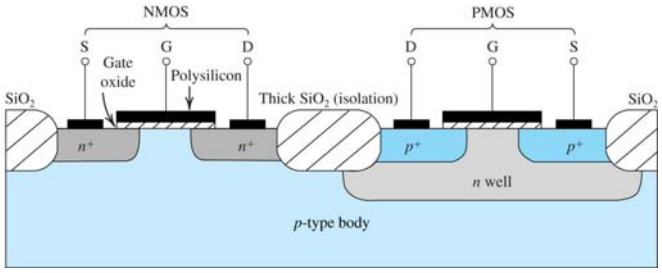


Figure 5.10 Cross section of a CMOS integrated circuit. Note that the PMOS transistor is formed in a separate *n*-type region, known as an *n* well. Another arrangement is also possible in which an *n*-type substrate (body) is used and the *n* device is formed in a *p* well. Not shown are the connections made to the *p*-type body and to the *n* well; the latter functions as the body terminal for the *p*-channel device.

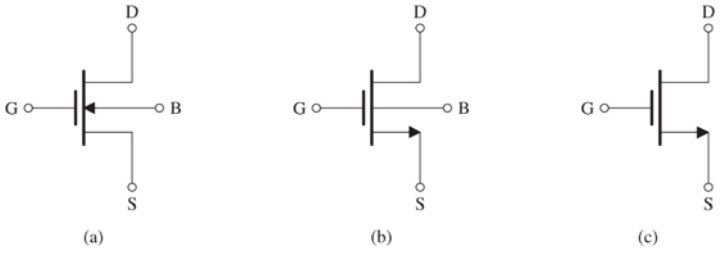
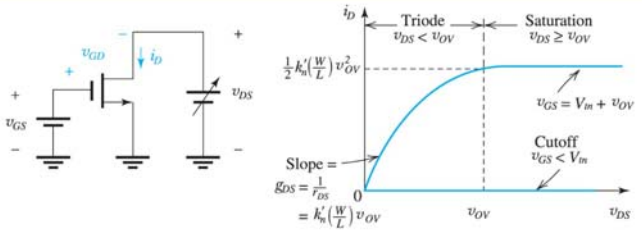


Figure 5.11 (a) Circuit symbol for the *n*-channel enhancement-type MOSFET. **(b)** Modified circuit symbol with an arrowhead on the source terminal to distinguish it from the drain and to indicate device polarity (i.e., *n* channel). **(c)** Simplified circuit symbol to be used when the source is connected to the body or when the effect of the body on device operation is unimportant.

Table 5.1 Regions of Operation of the Enhancement NMOS Transistor



- $v_{GS} < V_{tn}$: no channel; transistor in cutoff; $i_D = 0$
- $v_{GS} = V_{tn} + v_{OV}$: a channel is induced; transistor operates in the triode region or the saturation region depending on whether the channel is continuous or pinched off at the drain end;

Triode Region	*Saturation Region*
Continuous channel, obtained by: $v_{GD} > V_{tn}$	Pinched-off channel, obtained by: $v_{GD} \leq V_{tn}$
or equivalently: $v_{DS} < v_{OV}$	or equivalently: $v_{DS} \geq v_{OV}$
Then, $i_D = k_n'\left(\frac{W}{L}\right)\left[(v_{GS} - V_{tn})v_{DS} - \frac{1}{2}v_{DS}^2\right]$	Then $i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(v_{GS} - V_{tn})^2$
or equivalently, $i_D = k_n'\left(\frac{W}{L}\right)\left(v_{OV} - \frac{1}{2}v_{DS}\right)v_{DS}$	or equivalently, $i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)v_{OV}^2$

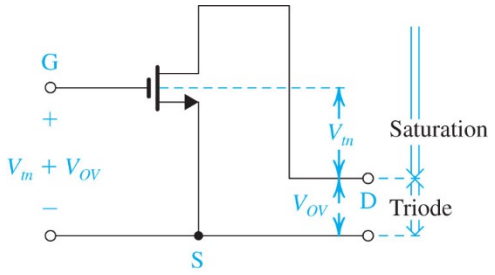


Figure 5.12 The relative levels of the terminal voltages of the enhancement NMOS transistor for operation in the triode region and in the saturation region.

Region of Operation --NMOS

Cut-off

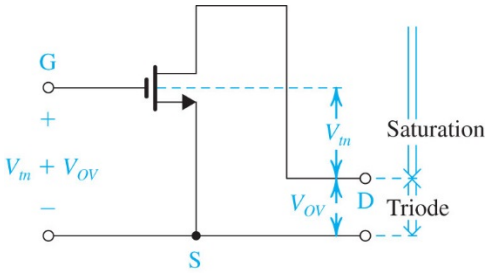
$$v_{GS} < V_{tn}$$

Saturation

$$v_{GS} > V_t$$
$$v_{DS} > v_{GS} - V_t$$
$$v_D - v_S > v_G - v_S - V_t$$
$$v_{GD} < V_t$$

Triode

$$v_{DS} < v_{OV}$$
$$v_{GD} > V_t$$



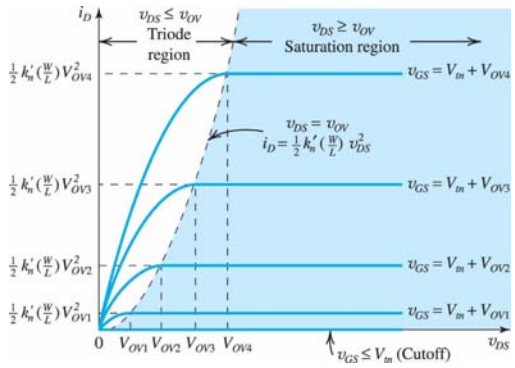
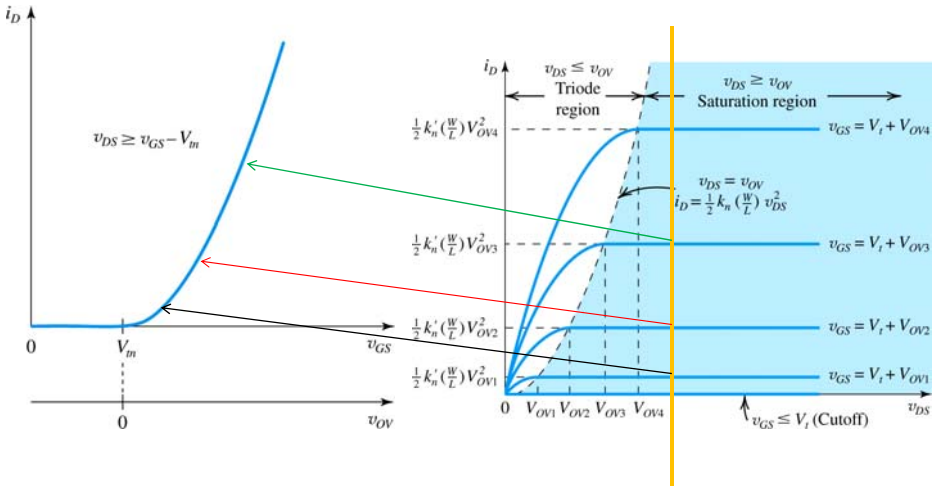


Figure 5.13 The $i_D - v_{DS}$ characteristics for an enhancement-type NMOS transistor.



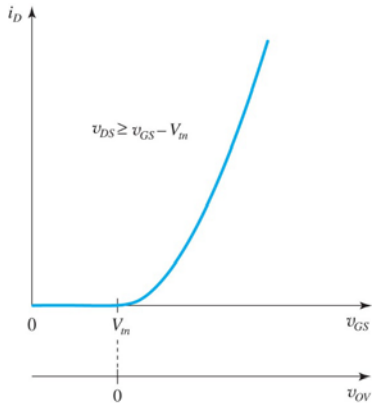
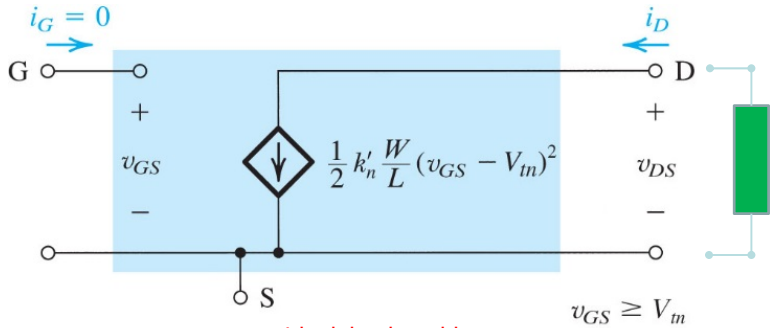


Figure 5.14 The i_D–v_{GS} characteristic of an NMOS transistor operating in the saturation region. The i_D–v_{OV} characteristic can be obtained by simply relabeling the horizontal axis, that is, shifting the origin to the point $v_{GS} = V_{tn}$.

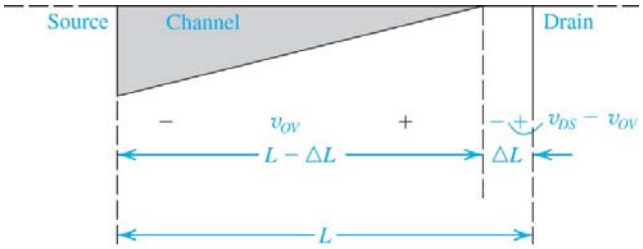


Operating in Saturation

Ideal, back to this point later

$$v_{GS} \geq V_{tn}$$
$$v_{DS} \geq v_{GS} - V_{tn}$$

Finite Output Resistance --Sat



Channel width modulation

- As v_{DS} increases, the channel *pinch off* moves away from the drain (L gets smaller).
- Voltage across the channel remains v_{ov}
- A voltage drop of $v_{DS} - v_{ov}$ appears across the small depletion region
- This voltage accelerates the electrons that reach the drain (increases current)

$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)V_{ov}^2$$

$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)V_{ov}^2(1+\lambda v_{DS})$$

$$r_o = \left[\frac{\partial i_D}{\partial v_{DS}}\right]^{-1}_{v_{GS}\ \text{constant}}$$

$$r_o = \left[\lambda \frac{k_n'}{2}\frac{W}{L}(V_{GS} - V_t)^2\right]^{-1}$$

$$r_o = \frac{1}{\lambda I_D} = \frac{V_A}{I_D}$$

$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)V_{ov}^2(1+\lambda v_{DS})$$

$i_D = 0$ when $v_{DS} = -1/\lambda = -V_A$

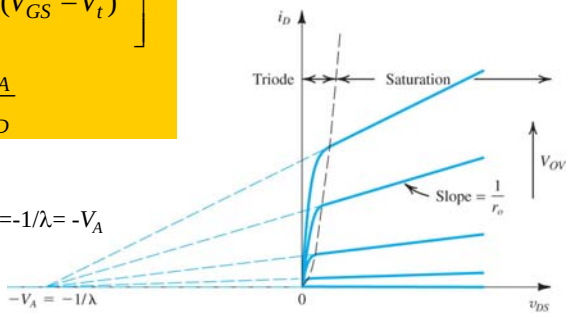


Figure 5.17 Effect of v_{DS} on i_D in the saturation region. The MOSFET parameter V_A depends on the process technology and, for a given process, is proportional to the channel length L.

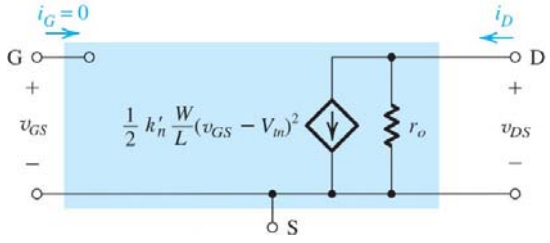


Figure 5.18 Large-signal, equivalent-circuit model of the n-channel MOSFET in saturation, incorporating the output resistance r_o. The output resistance models the linear dependence of i_D on v_{DS} and is given by Eq. (5.27).

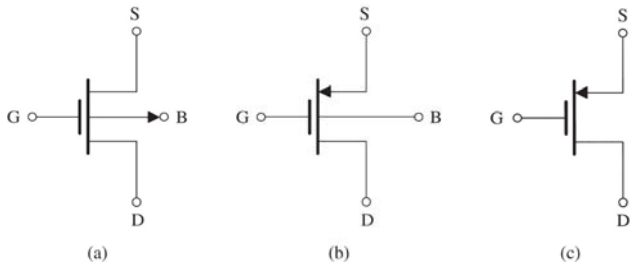
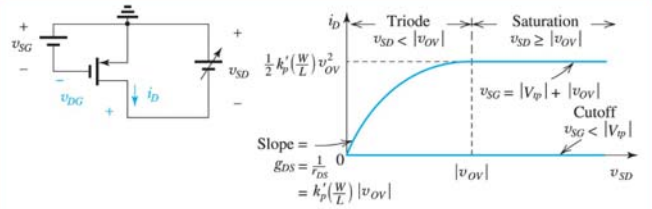


Figure 5.19 (a) Circuit symbol for the *p*-channel enhancement-type MOSFET. **(b)** Modified symbol with an arrowhead on the source lead. **(c)** Simplified circuit symbol for the case where the source is connected to the body.

Table 5.2 Regions of Operation of the Enhancement PMOS Transistor



- $v_{SG} < |V_{tp}|$: no channel; transistor in cutoff; $i_D = 0$
- $v_{SG} = |V_{tp}| + |v_{OV}|$: a channel is induced; transistor operates in the triode region or in the saturation region depending on whether the channel is continuous or pinched off at the drain end;

Triode Region	*Saturation Region*
Continuous channel, obtained by: $v_{DG} > \|V_{tp}\|$	Pinched-off channel, obtained by: $v_{DG} \leq \|V_{tp}\|$
or equivalently $v_{SD} < \|v_{OV}\|$	or equivalently $v_{SD} \geq \|v_{OV}\|$
Then $i_D = k'_p\left(\frac{W}{L}\right)\left[(v_{SG} - \|V_{tp}\|)v_{SD} - \frac{1}{2}v_{SD}^2\right]$	Then $i_D = \frac{1}{2}k'_p\left(\frac{W}{L}\right)(v_{SG} - \|V_{tp}\|)^2$
or equivalently $i_D = k'_p\left(\frac{W}{L}\right)\left(\|v_{OV}\| - \frac{1}{2}v_{SD}\right)v_{SD}$	or equivalently $i_D = \frac{1}{2}k'_p\left(\frac{W}{L}\right)v_{OV}^2$

PMOS

Cut-off

$$v_{SG} < |V_{tp}|$$

Saturation

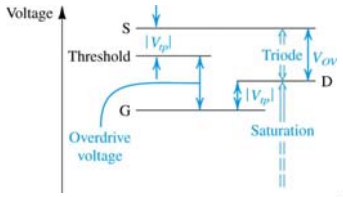
$$v_{DG} \leq |V_{tp}|$$

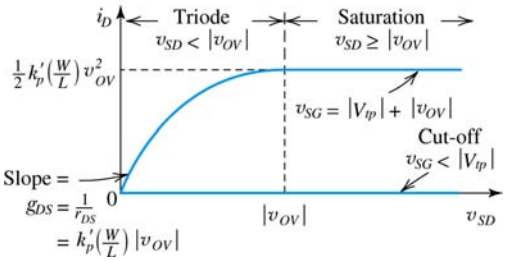
$$v_{SD} \geq |v_{OV}|$$

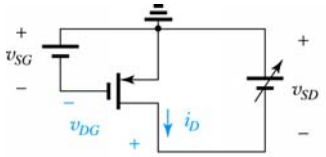
Triode

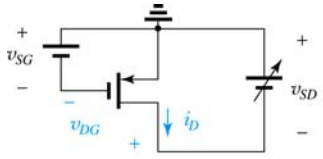
$$v_{SD} < |v_{OV}|$$

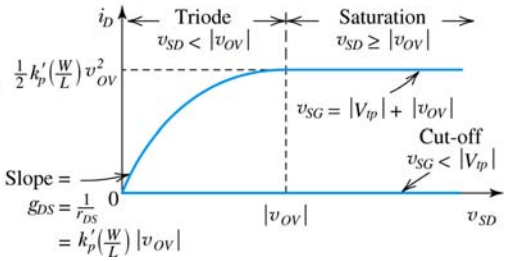
$$v_{DG} > |V_t|$$

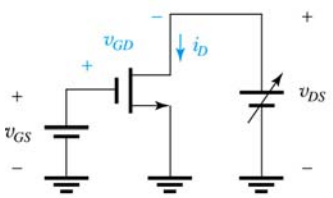


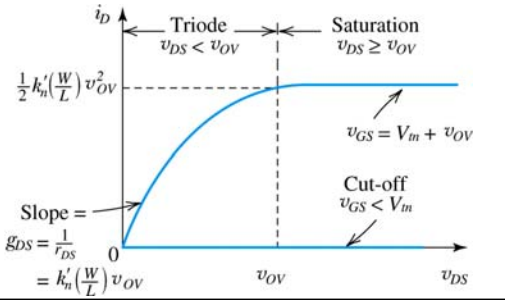












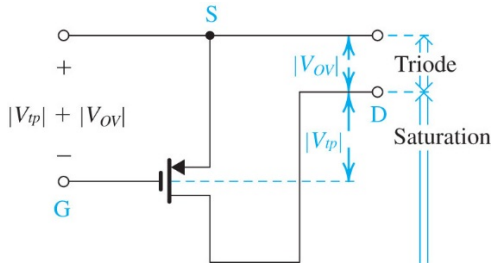
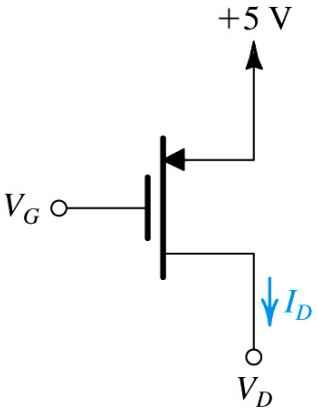


Figure 5.20 The relative levels of the terminal voltages of the enhancement-type PMOS transistor for operation in the triode region and in the saturation region.

EXAMPLE



V_{tp} = -1 V, K_p'=60 μA/v², W/L=10

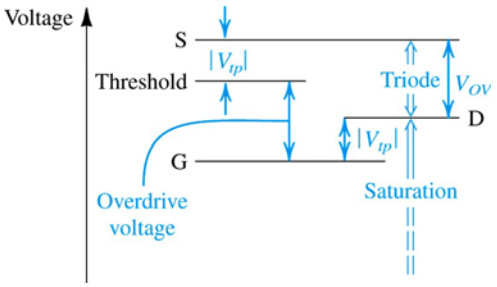


Figure E5.7

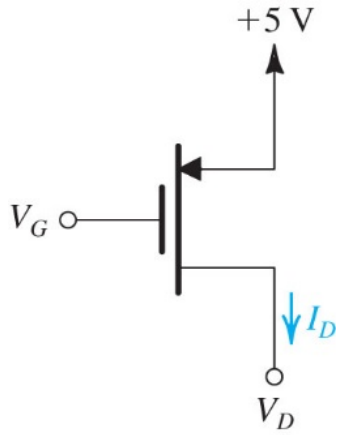


Figure E5.7

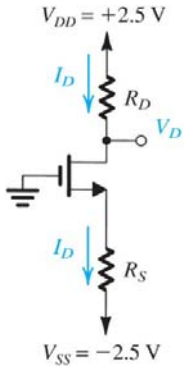
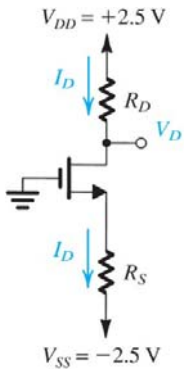


Figure 5.21 Circuit for Example 5.3.

Example

- Redesign the previous circuit for:

1. V_{DD}=- V_{SS}=2.5V
2. V_t=1V
3. $\mu_n C_{ox}$=60μA/V2. W/L=120/3
4. I_D=0.3mA, V_D=+0.4V



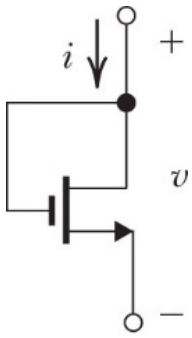


Figure 5.22

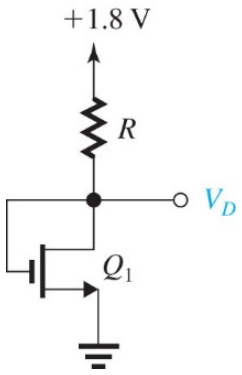


Figure E5.9

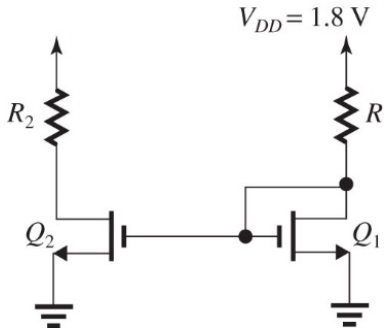


Figure E5.10

