EECS4210 Architecture & Hardware for DSP

Chapter 6

Activity

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Activity 1

In the signal-flow graph (SFG) in Fig. a, the computation time for each node is assumed to be 1 u.t.

(1) Calculate the critical path computation time.

(2) The critical path has been reduced to 2 u.t. by inserting 3 extra latches as shown in Fig. b. Is this a valid pipelining? If not, how to get a valid one.

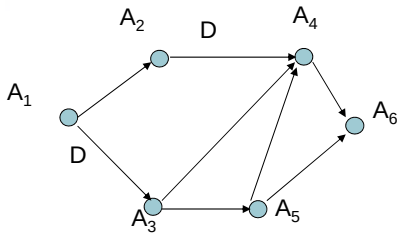


Fig. a

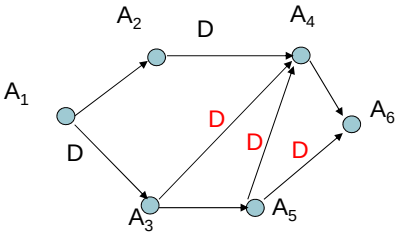
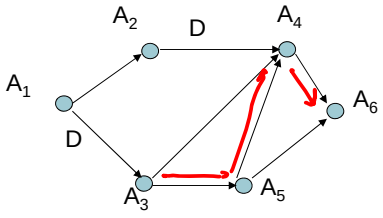


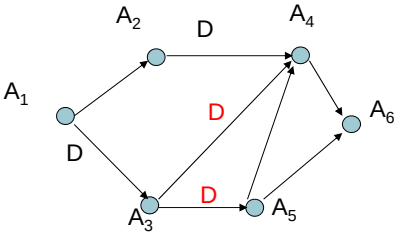
Fig. b

Solution Activity 1

Critical Path =4 u.t.



Critical Path =3 u.t.



Critical Path =2 u.t.

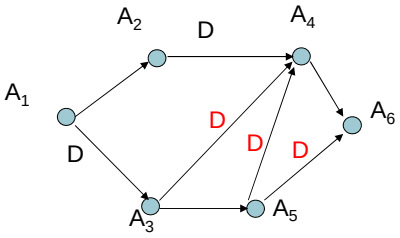


Fig. b

Solution Activity 1

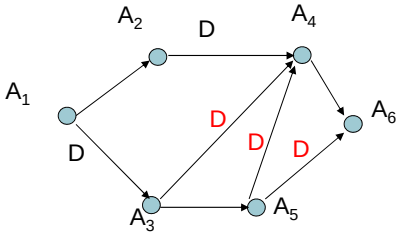
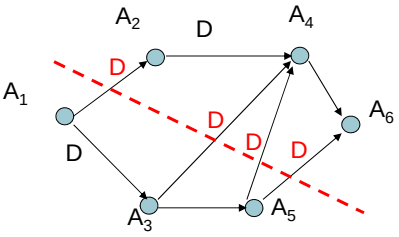


Fig. b

Not a valid pipelining implementation



A valid pipelining implementation