1.4

a. 1280×1024 pixels $= 1{,}310{,}720$ pixels $=> 1{,}310{,}720 \times 3 = 3{,}932{,}160$ bytes/frame.

b. $3{,}932{,}160$ bytes $\times$ (8 bits/byte) /100E6 bits/second $= 0.31$ seconds

1.5

a. performance of P1 (instructions/sec) $= 3 \times 10^9/1.5 = 2 \times 10^9$

performance of P2 (instructions/sec) $= 2.5 \times 10^9/1.0 = 2.5 \times 10^9$

performance of P3 (instructions/sec) $= 4 \times 10^9/2.2 = 1.8 \times 10^9$

b. $\text{cycles(P1)} = 10 \times 3 \times 10^9 = 30 \times 10^9$

$\text{cycles(P2)} = 10 \times 2.5 \times 10^9 = 25 \times 10^9$

$\text{cycles(P3)} = 10 \times 4 \times 10^9 = 40 \times 10^9$

No. instructions(P1) $= 30 \times 10^9/1.5 = 20 \times 10^9$

No. instructions(P2) $= 25 \times 10^9/1 = 25 \times 10^9$

No. instructions(P3) $= 40 \times 10^9/2.2 = 18.18 \times 10^9$

c. $CPI_{new} = CPI_{old} \times 1.2$, then CPI(P1) $= 1.8$, CPI(P2) $= 1.2$, CPI(P3) $= 2.6$

$f =$ No. instr. $\times$ CPI/time, then

$f(P1) = 20 \times 10^9 \times 1.8/7 = 5.14$ GHz

$f(P2) = 25 \times 10^9 \times 1.2/7 = 4.28$ GHz

$f(P1) = 18.18 \times 10^9 \times 2.6/7 = 6.75$ GHz

1.6

a. Class A: 10^5 instr. Class B: 2×10^5 instr. Class C: 5×10^5 instr. Class D: 2×10^5 instr.

Time = No. instr. $\times$ CPI/clock rate

Total time P1 $= (10^5 + 2 \times 10^5 \times 2 + 5 \times 10^5 \times 3 + 2 \times 10^5 \times 3)/(2.5 \times 10^9) = 10.4 \times 10^{-4}$ s

Total time P2 $= (10^5 \times 2 + 2 \times 10^5 \times 2 + 5 \times 10^5 \times 2 + 2 \times 10^5 \times 2)/(3 \times 10^9) = 6.66 \times 10^{-4}$ s

CPI = CPU Time x Clock Rate / Instruction Count

CPI(P1) $= 10.4 \times 10^{-4} \times 2.5 \times 10^9/10^6 = 2.6$

CPI(P2) $= 6.66 \times 10^{-4} \times 3 \times 10^9/10^6 = 2.0$

b. clock cycles(P1) $= 10^5 \times 1 + 2 \times 10^5 \times 2 + 5 \times 10^5 \times 3 + 2 \times 10^5 \times 3$
$= 26 \times 10^5$

clock cycles(P2) $= 10^5 \times 2 + 2 \times 10^5 \times 2 + 5 \times 10^5 \times 2 + 2 \times 10^5 \times 2$
$= 20 \times 10^5$

1.7

a. $CPI = T_{exec} \times f/\text{No. instr.}$

Compiler A CPI = 1.1

Compiler B CPI = 1.25

b. Clock Rate = No. of Instructions x CPI / CPU Time

$f_B/f_A = (\text{No. instr.(B)} \times CPI(B))/(\text{No. instr.(A)} \times CPI(A)) = 1.37$

c. For a processor, clock rate remains same for all compilers

T_A / T_{new} = No. of Instructions_A x CPI_A / No. of $\text{Instructions}_{new}$ x CPI_{new}

$T_A/T_{new} = 1.67$
$T_B/T_{new} = 2.27$

1.8

1.8.1 The dynamic power for a pulse during the logic transition of 0 → 1 → 0 or 1 → 0 → 1.
Power = C x Voltage^2 x Frequency
The dynamic power for a single transition during the logic transition of 0 → 1 or 1 → 0.
Power = 2 x C x Voltage^2 x Frequency
Pentium 4: C = 2 x P / V^2 x f = 2 x 90 / 1.25^2 x $3.6\text{x}10^9$ = 3.2 x 10^{-8} F
Core i5 Ivy Bridge: C = 2 x P / V^2 x f = 2 x 40 / 0.9^2 x $3.4\text{x}10^9$ = 2.9 x 10^{-8} F

1.8.2 Pentium 4: 10/100 = 10%

Core i5 Ivy Bridge: 30/70 = 42.9%

1.10

1.10.1 die area_{15cm} = wafer area/dies per wafer = $pi*7.5^2 / 84 = 2.10\ cm^2$

$\text{yield}_{15cm} = 1/(1+(0.020*2.10/2))^2 = 0.9593$

die area_{20cm} = wafer area/dies per wafer = $pi*10^2/100 = 3.14\ cm^2$

$\text{yield}_{20cm} = 1/(1+(0.031*3.14/2))^2 = 0.9093$

1.10.2 $\text{cost/die}_{15cm} = 12/(84*0.9593) = 0.1489$

$\text{cost/die}_{20cm} = 15/(100*0.9093) = 0.1650$

1.10.3 die area_{15cm} = wafer area/dies per wafer = $pi*7.5^2/(84*1.1) = 1.91\ cm^2$

$\text{yield}_{15cm} = 1/(1 + (0.020*1.15*1.91/2))^2 = 0.9575$

die area_{20cm} = wafer area/dies per wafer = $pi*10^2/(100*1.1) = 2.86\ cm^2$

$\text{yield}_{20cm} = 1/(1 + (0.03*1.15*2.86/2))^2 = 0.9082$