York University

Lassonde School of Engineering

Dept. of Electrical Engineering and Computer Science Fall 2015

EECS4201	Midterm	Computer Architecture
Tuesday, Oct. 27 th , 2015		10:00 – 11:15
Last Name	First name	
ID		

Instructions to students:

Answer all questions.

Marks are shown in front of each question number.

Show your work

Be neat and clean while drawing your logic, block, or state diagrams.

This examination consists of 4 questions

Problem	Points
1	/4
2	/6
3	/9
4	/5
Total	/24

Problem 1 (4 points)

Can instructions in Tomasulo's algorithm finish execution out of order?

If yes, discuss how we can deal with write after write if the second write finishes before the first one does?

If No, explain the mechanism by which we enforce in-order completion of the instructions

Problem 2 (6 points)

Consider a 2-bit branch predictor (initially set to deep NT), how many misses results when executing the following branch patterns.

What if we consider 1-bit predictor

Problem 3 (9 points)

For the shown loop below, and a standard MIPS pipeline (EX stage for ADD.D takes 3 cycles, EX stage for any other instruction takes 1 cycle, branches are resolved in ID stage):

Loop: L.D F2, 100(R1) L.D F4, 500(R1) ADD.D F6, F2, F4 ADD.D F8, F6, F2 S.D F8, 100(R1) DADDUI R1, R1, #4 DADDUI R2, R2,#-1 BNEZ R2, Loop

a) How many cycles per iteration, and how many stalls per iteration?

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b) Shuffle instructions around to minimize stalls. You may change offsets if necessary. How many cycles per iteration does modified loop take and how many stalls are left?

c) Unroll the loop twice (so that there are total of two iterations in the unrolled code) and rearrange the code so that to minimize stalls. How many cycles does one iteration of the original loop takes now?

Problem 4 (4 points)

Briefly explain how global correlating branch predictor works?