EECS3611 Analog Integrated Circuit Design

Chapter 1

Introduction

EECS3611 Analog Integrated Circuit Design

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- Course Web
  https://wiki.eecs.yorku.ca/course_archive/2016-17/W/3611/
- Schedule:
  - Lectures: PSE321, Mon. & Wed. 4:00pm – 5:30pm
  - Labs@BEL 334, Thur. 6:30pm-9:30pm,
- Office hours:
  Wed. 2:00-3:30pm@LAS1012C (starting Feb. 1, 2017)

EECS3611 Analog Integrated Circuit Design

- Textbook

Design of Analog CMOS Integrated Circuits
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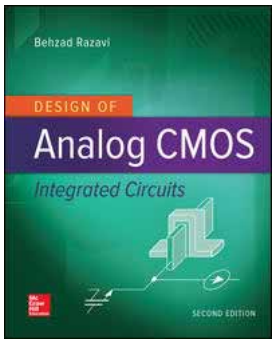

Grade Components

- Assignment: 10%
- Quiz: 15% (3 quizzes in class)
- Lab: 25%
  - 8 lab sessions
  - Starts on Jan. 26 (week 4, tentative)
  - Assessment based on lab report and design project.
- Midterm 20%
- Final 30%

LAB

- Lab will be at BEL 334
- Lab contains two parts
  - Part 1 is for learning of EDA tool (i.e. Cadence), circuit simulation, and layout.
  - Part 2 is for a design project.
- Maintain a laboratory book or journal for all lab sessions. It must be signed by the TA before you leave the lab.

Topics covered

- Introduction to analog design
- Basic MOS device physics
- Single state amplifiers
- Layout and design rules
- Differential amplifiers
- Passive and active current mirrors
- Frequency response of amplifiers
- Noise
- Feedback
- Operational amplifiers

Learning Outcomes

- After successful completion of the course, students are expected to be able to:
  - To analyze the characteristics of basic analog integrated circuits
  - To formulate the behavior of basic analog circuits by inspection
  - To perform circuit simulation using computer-aided tool
  - To draw layout based on given design rules

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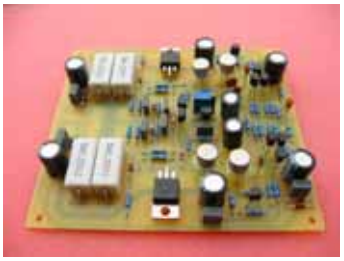
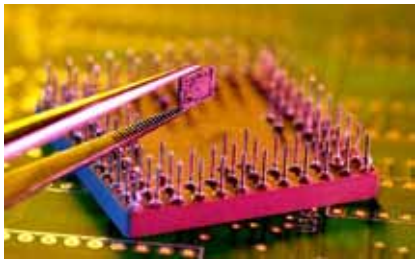
Introduction

Discrete Component and Integrated Circuits

- Discrete component circuit (in EECS2210) consists of different active components (transistors) and passive components (capacitors, resistors and inductors).
- Integrated circuit (this course) is a monolithic circuit fabricated on a semiconductor substrate. It mainly consists of transistors with limited number of resistors and small value capacitors.



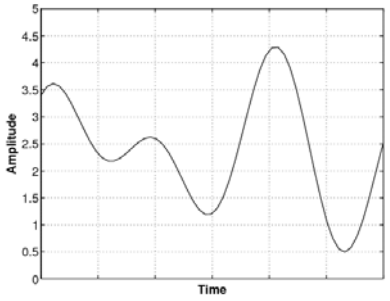


Discrete Component and Integrated Circuits

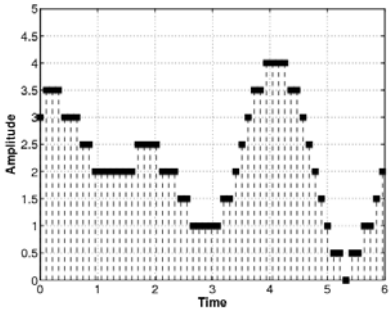
- Discrete component circuit:
  - Both active and passive components are available.
  - Most are AC coupled circuit to isolate the DC biasing points of different devices.
  - Low device density, high power consumption.
- Integrated circuit:
  - Mainly transistors, as resistors and capacitors occupy larger chip area.
  - Most are DC coupled circuit.
  - High device density, low power consumption.
  - High speed.

Analog and Digital

- Analog signal: Continuous in time and amplitude
- Digital signal: discrete in time and amplitude

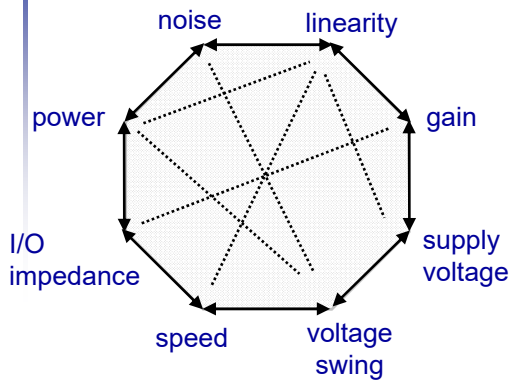


Analog signal



Digital signal

Design of Analog and Digital Circuits



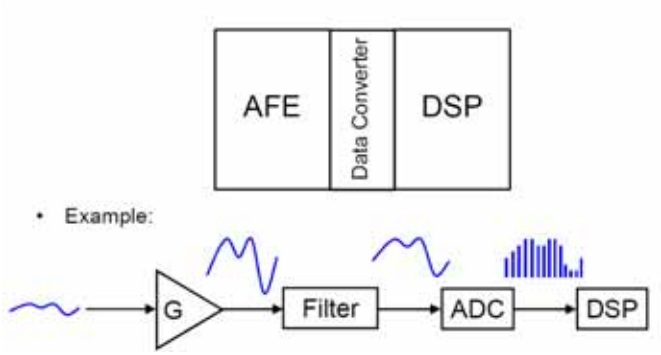
Analog circuit

Digital circuit

Multi trade-offs in analog design make it very complex.

Why Analog?

- Most of the physical signals are analog in nature
- Need analog circuits to interface with physical world



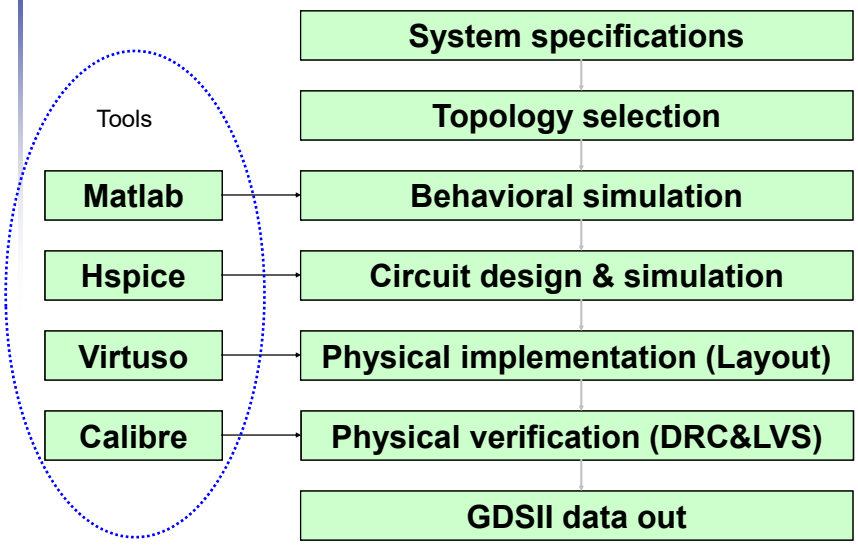
Why CMOS?

- CMOS is now dominate the digital IC market:
  - Simple device structure, low fabrication cost.
  - Simple circuit for digital gates.
  - Advancement in CMOS technology.
  - Scalable and high integration density.
- The demands for smaller and cheaper device, i.e. monolithic circuit and System-on-Chip (SOC), drive analog IC to CMOS technology.
  - To integrate analog and digital circuits into one chip.
  - To reduce the cost.
- Analog IC is moving to CMOS technologies, especially for low voltage and low power applications.

Passive Devices in CMOS

- Resistor in CMOS:
  - Diffusion resistor: sheet resistance 100 Ω/□ to 200Ω/□
  - Poly silicon resistor: sheet resistance 20 Ω/□ to 80Ω/□
  - Well resistor: ~10kΩ/□
- Capacitor in CMOS:
  - PIP (poly-insulator-poly) capacitance: high linearity, unit capacitance <1fF/μm^2
  - MIM (metal-insulator-metal) capacitance: high linearity, unit capacitance ~1fF/μm^2
  - MOS capacitance: Use C_G as capacitance– voltage dependence
- Large process variation: ±20%.
- Passive devices occupy larger silicon area

Analog IC Design Flow



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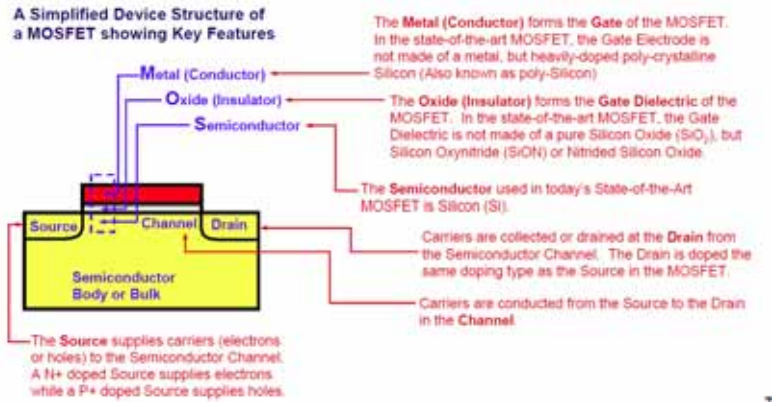
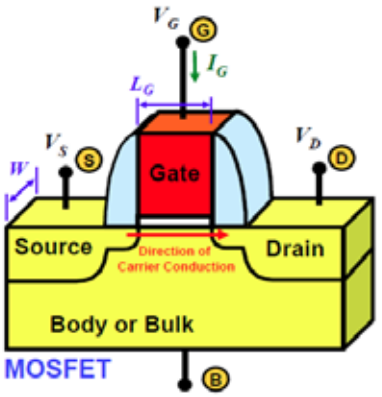
Review of MOSFET

MOSFET

- MOSFET stands for Metal-Oxide-Semiconductor Field-Effect Transistor.
- A MOSFET comprises a Metal-Oxide-Semiconductor stack



MOSFET: 3D Structure



There are 4 terminals:
- G Gate. Gate Voltage V_G.
- S Source. Source Voltage V_S.
- D Drain. Drain Voltage V_D.
- B Body or Bulk. Body Voltage V_B.

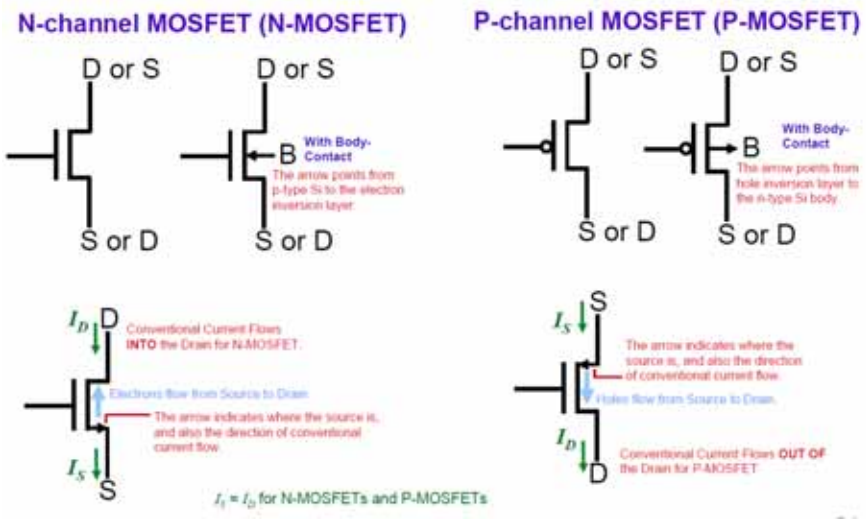
Note that the MOSFET is structurally symmetrical such that the source and drain can be interchanged.

Two Types of MOSFETs

	Source or Drain	Body	Charge Carriers
n-Channel MOSFET	n^+ Si	p-Si	Electrons
p-Channel MOSFET	p^+ Si	n-Si	Holes

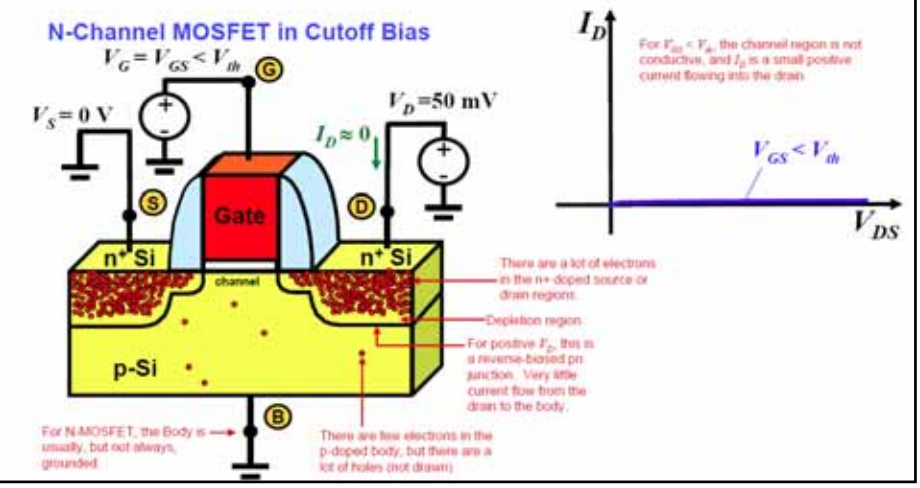
MOSFET Symbols

- Two types of MOSFETs



NMOS: Cutoff or Turned-Off

- When V_{GS} is less than a Threshold Value V_{th} (Threshold Voltage), there are little charge carriers (electrons in p-type Si) in the channel region.
- Even though there can be a voltage V_{DS} applied between the drain and the source, little electrons flow from the source to the drain.



NMOS: Linear Region

- When $V_{GS} > V_{th}$, the gate causes the channel to be filled with electrons (from the source) and the channel is conductive. This layer of electrons forms an inversion layer.
- When a positive V_{DS} is applied between the drain and the source, the electrons flow from the source to the drain.

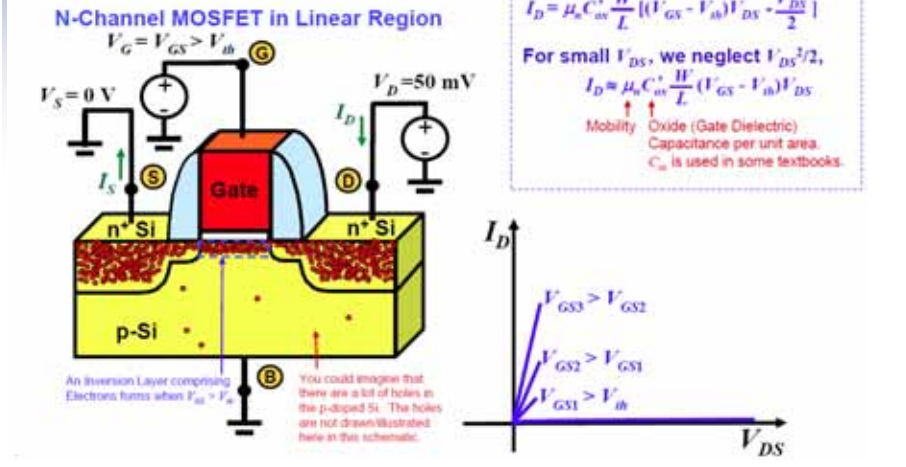
In the Linear Region, I_D is given by

$$I_D = \mu_n C'_{ox} \frac{W}{L}\left[(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right]$$

For small V_{DS}, we neglect $V_{DS}^2/2$,

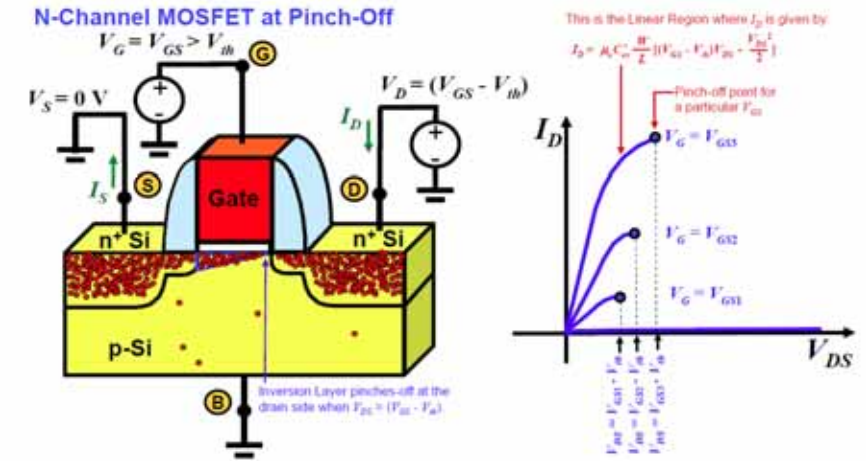
$$I_D \approx \mu_n C'_{ox} \frac{W}{L}(V_{GS} - V_{th})V_{DS}$$

Mobility. Oxide (Gate Dielectric) Capacitance per unit area. C_{ox} is used in some textbooks.



NMOS: Pinch-Off [$V_{DS}=V_{GS}-V_{th}$]

- For each applied V_{GS} (which is greater than V_{th}), the applied V_{DS} can be increased, and more drain current I_D flows.
- When V_{DS} is equal to $(V_{GS} - V_{th})$, the inversion layer pinches off at the drain side.



NMOS: Saturation [$V_{DS}\geq V_{GS}-V_{th}$]

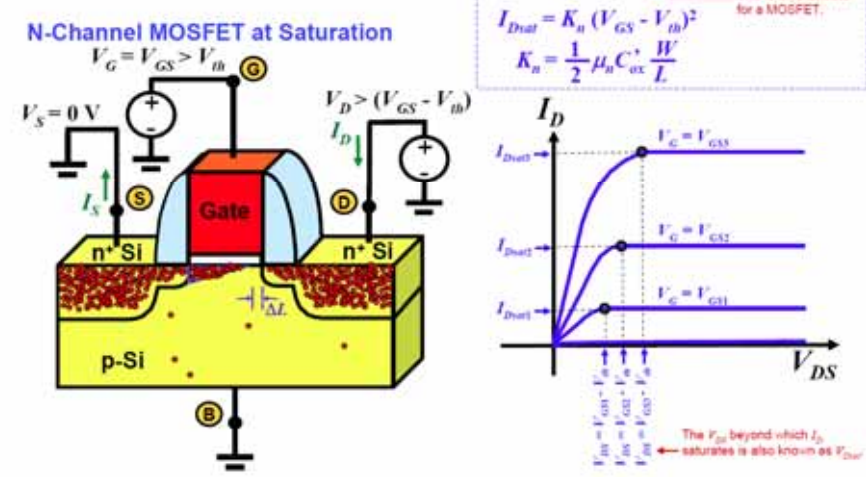
- When V_{DS} is increased beyond $(V_{GS} - V_{th})$, i.e. beyond the point where pinch-off occurs, the drain current I_D saturates at a value I_{Dsat}.
- The saturation drain current I_{Dsat} is given by

$$I_{Dsat} = \frac{1}{2}\mu_n C_{ox}' \frac{W}{L} (V_{GS} - V_{th})^2$$

This is a constant K for a MOSFET.

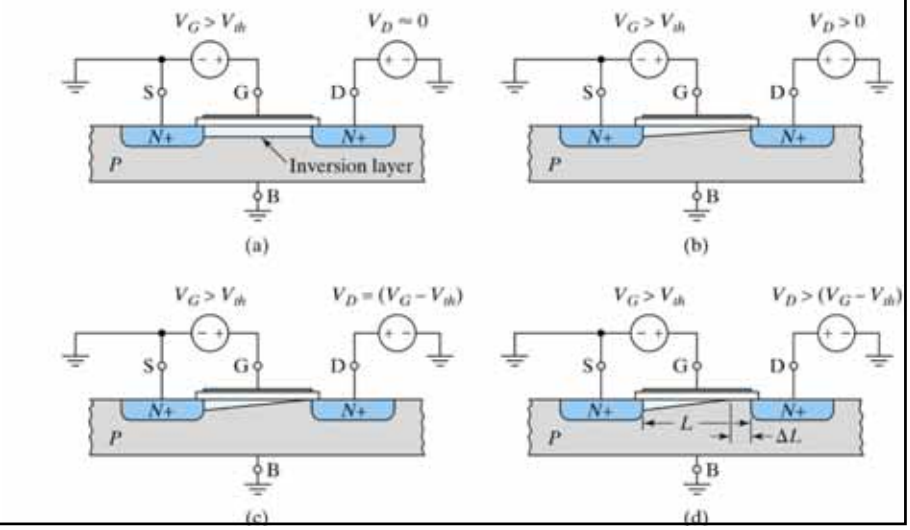
$$I_{Dsat} = K_n (V_{GS} - V_{th})^2$$

$$K_n = \frac{1}{2}\mu_n C_{ox}' \frac{W}{L}$$

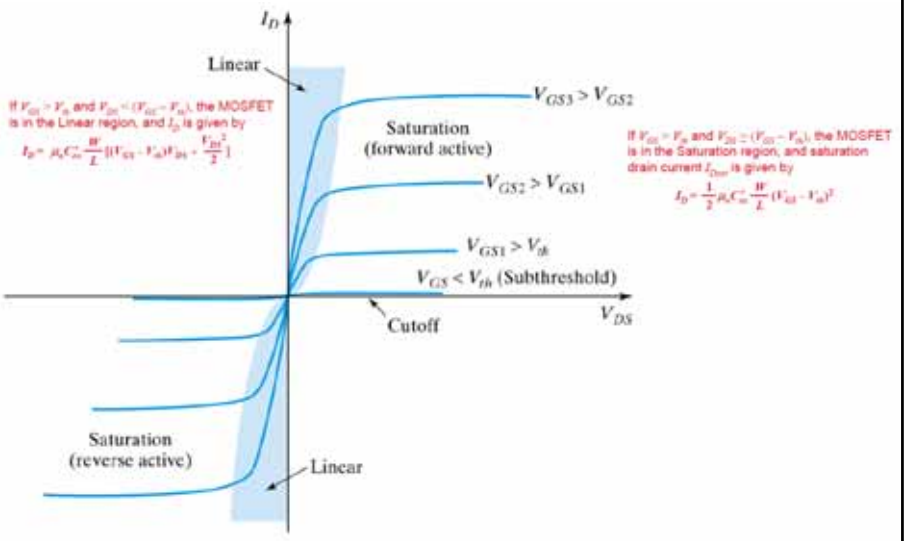


NMOS Operation

The charge in the inversion layer as a function of V_D: (a) small values of V_D, (b) larger values of V_D, (c) pinch-off, and (d) V_D greater than pinch-off.

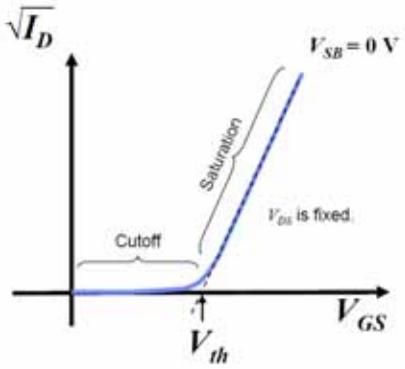


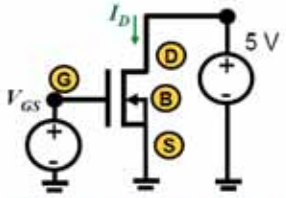
NMOS: I_D-V_{DS} Characteristics



NMOS: I_D-V_{GS} Characteristics

- In the Saturation region [$V_{GS} > V_{th}$ and $V_{DS} \geq (V_{GS} - V_{th})$], we have $I_{Dsat} = K_n (V_{GS} - V_{th})^2$
- Taking square root, $\sqrt{I_{Dsat}} = \sqrt{K_n}\cdot(V_{GS} - V_{th})$
- By measuring and obtaining $\sqrt{I_D}$ and plotting it with respect to V_{GS}, we can extract K_n (from slope) and V_{th} (from horizontal intercept):





- For this N-MOSFET, Body is tied to Source, i.e. both are grounded. $V_B = 0$ V.
- In the above circuit, $V_{SB} = 0$, and the threshold voltage measured is also denoted by V_{th0}.

Body Effect

- In circuits, it may not always be possible to keep V_{BS} for a transistor at 0 V.
- When V_{BS} deviates from 0 V, the threshold voltage of the transistor varies. We need to account for this effect.
- The threshold voltage with body effect is given by

$$V_{th} = V_{th0} + \gamma\left[\sqrt{|2\phi_f| + |V_{SB}|} - \sqrt{|2\phi_f|}\right]$$

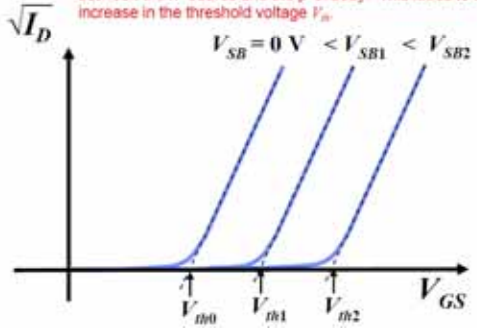
Body effect parameter

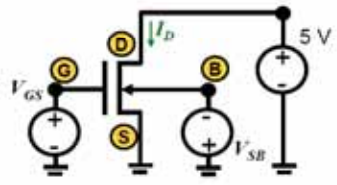
Doping concentration in body
Intrinsic carrier concentration in Silicon

$\phi_f = V_T \ln(N_A/n_i)$ for p-type Si body (N-MOSFET)

kT/q, which is 25 mV at 300 K.

Increasing V_{SB} increases the reverse bias for the pn junction between the n+ source and the p-Si body. This leads to an increase in the threshold voltage V_{th}.

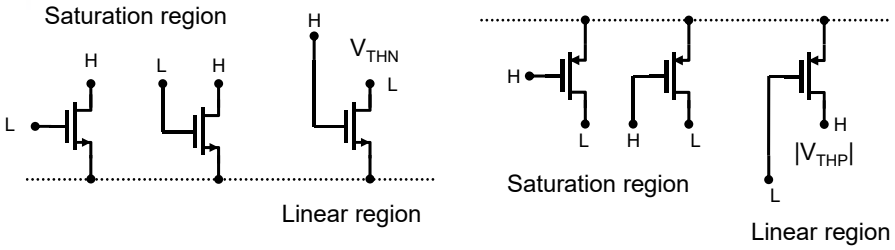




For this N-MOSFET, the Body or Bulk Bias V_B is varied.

Summary: Region of Operation

- Cut off region: $V_{GS} < V_{TH}$
- Linear region: $V_{GS} > V_{TH}$, $V_{DS} \leq V_{GS}$-V_{TH}
- Saturation region: $V_{GS} > V_{TH}$, $V_{DS} > V_{GS}$-V_{TH}

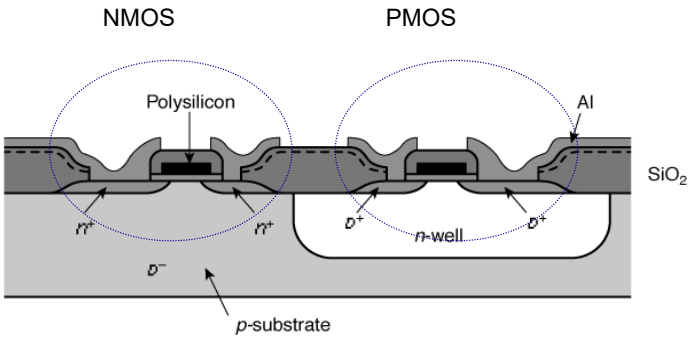


MOSFET: CMOS

- CMOS stands for Complementary Metal-Oxide-Semiconductor
- Containing PMOS and NMOS transistors
- P-channel device has opposite relative voltages, has P+ source drains, and n-type substrate. Both NMOS and PMOS devices are used in CMOS technology.
- P-channel device produces less transconductance for similar dimension and current compared to n-channel due to lower mobility of holes.

MOSFET: CMOS

- Cross section of a NMOS and a PMOS FET in a CMOS technology.



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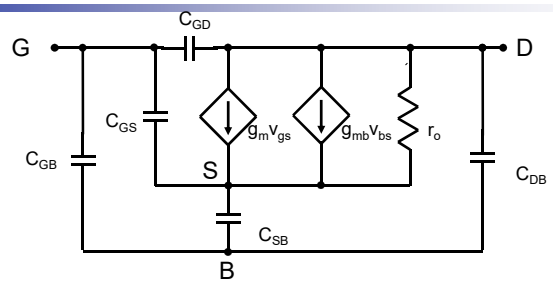
Circuit Models

Models for Design

- Transistor is modeled using basic circuit components.
- Two types of models: large signal model and small signal model
  - Large signal model – large signal low frequency, such as DC bias points.
  - Small signal model – small signal and parameters such as gain and frequency response of an analog circuit.

MOSFET Model for Design



A transistor is modeled by using four major components:

- A voltage controlled current source to model the transconductance g_m.
- Output resistance r_o.
- A voltage controlled current source to model the back gate transconductance g_{mb}.
- Parasitic capacitance C_{xx}.

Transistor DC Modeling

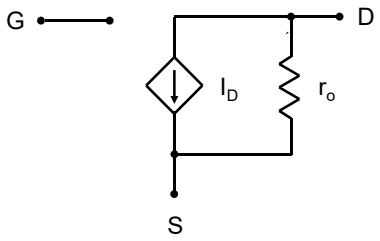
$$I_D = 0 \qquad for\ V_{GS} \le V_{TH}$$

$$I_D = \mu C_{ox} \frac{W}{L}\left[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2 \right] \qquad for\ V_{GS} > V_{TH},\ V_{DS} \le V_{GS}-V_{TH}$$

$$I_D = \frac{1}{2}\mu C_{ox} \frac{W}{L}(V_{GS} - V_{TH})^2 (1+\lambda V_{DS}) \qquad for\ V_{GS} > V_{TH},\ V_{DS} > V_{GS}-V_{TH}$$

where $V_{GS} - V_{TH} = V_{OD} = V_{DSAT}$.

$$V_{TH} = V_{TH0} + \gamma[\sqrt{|2\Phi_F + V_{SB}|} - \sqrt{|2\Phi_F|}]$$



Small Signal (AC) Model for Circuit Analysis

- The model shown earlier is good for transistor DC bias point calculation.
- For AC analysis, a simple small signal model is developed. In this analysis, a small AC signal *v* is superimposed on normal DC biases.
- In notation, AC signals will use all small letters, DC all capitals and total voltage with AC and DC components added will use mixed case throughout this course. For example, V_{OUT} is a DC voltage, v_{out} is an AC voltage and V_{out} is the total voltage .

Transconductance

- The effect of gate voltage controlling the drain current is modeled by transconductance

$$g_m = \frac{\partial I_D}{\partial V_{GS}}$$

- Hence this g_m models how drain current will change with change in gate voltage.
- The transconductance is the most important parameter of a transistor in analog circuit design.
- This effect is modeled as a voltage controlled current source between drain and source.

Transconductance

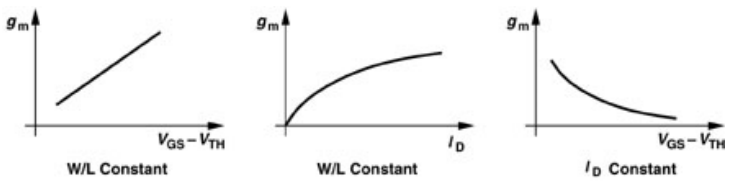
- In the linear region, the transconductance of a MOSFET is

$$g_m = \mu C_{ox} \frac{W}{L} V_{DS}$$

clearly indicating a drop with decreasing V_{DS}.

- In the saturation region

$$g_m = \mu C_{ox} \frac{W}{L}(V_{GS} - V_{TH}) = \sqrt{2\mu C_{ox} \frac{W}{L} I_D} = \frac{2I_D}{V_{GS} - V_{TH}}$$



Output Conductance

- The effect of the drain voltage is modeled using the output conductance

$$g_d = \frac{\partial I_D}{\partial V_{DS}}$$

- This models how I_D changes when the V_{DS} changes. Since we want only input voltage to control I_D and not the output voltage, ideally, this should be zero.
- Hence in saturation region using I_D expression:

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1+\lambda V_{DS}) \rightarrow g_d = \frac{\partial I_D}{\partial V_{DS}} \approx \lambda I_D$$

- This effect is captured as a resistance called output resistance:

$$r_o = \frac{1}{g_d} = \frac{1}{\lambda I_D}$$

Back Gate Transconductance

- The effect of body bias or bulk voltage is modeled using body or back gate transconductance.

$$g_{mb} = \frac{\partial I_D}{\partial V_{BS}}$$

- Hence this value is mainly determined by γ. This effect is captured as a dependent current source circuit element between drain and source.

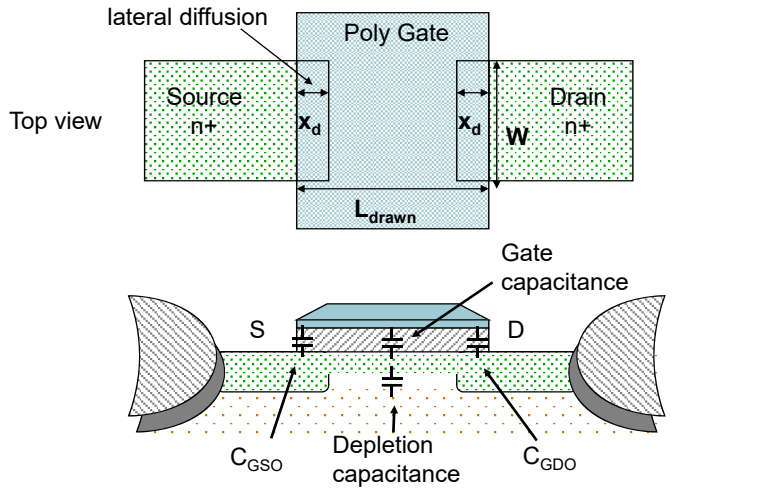
$$g_{mb} = \frac{\partial I_D}{\partial V_{BS}} = g_m \frac{\gamma}{2\sqrt{2\Phi_F + V_{SB}}} = \eta g_m$$

- Normally the back gate transconductance is 20% of the front gate transconductance, i.e. η=0.2.

MOSFET Capacitance

- The fundamental mode of MOSFET operation is through charge which is modeled through 3 non-linear bias dependent capacitances C_{GS}, C_{GD} and C_{GB} .
- In addition, there are three linear overlap capacitances.
  - C_{GSO} : Gate to source overlap capacitance per meter of channel width. This and drain overlap capacitance are independent of length L as they are associated with edge effects.
  - C_{GDO} : Similar to drain counterpart.
  - C_{GBO} : Gate to bulk overlap capacitance per meter of channel length and is associated with edge effects at the width ends of the gate area.

MOS Structure Overlap Capacitance



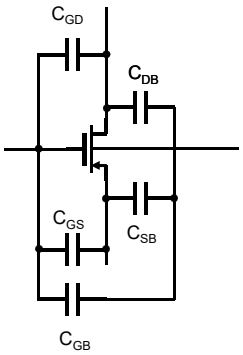
Overlap capacitance (linear): $C_{GSO} = C_{GDO} = C_{OV} \cdot W$

Total Gate Capacitance

- Total gate capacitance in cut-off region:
  - C_{GB} is WLC_{ox} in series with C_d
  - C_d is the depletion region capacitance

$$C_d = WL\sqrt{\frac{q\xi_{si}N_A}{4\Phi_F}}$$

$$C_{GS} = C_{GSO}$$
$$C_{GD} = C_{GDO}$$
$$C_{GB} = \frac{(WLC_{ox})Cd}{(WLC_{ox}) + Cd}$$



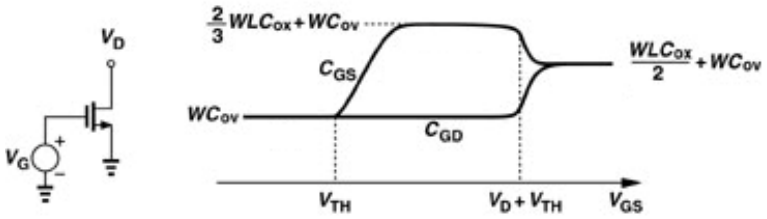
- In linear region:

$$C_{GS} = C_{GSO} + \frac{1}{2}WLC_{ox}$$
$$C_{GD} = C_{GDO} + \frac{1}{2}WLC_{ox}$$
$$C_{GB} = 0$$

- In saturation region:

$$C_{GS} = C_{GSO} + \frac{2}{3}WLC_{ox}$$
$$C_{GD} = C_{GDO}$$
$$C_{GB} = 0$$

Total Gate Capacitance

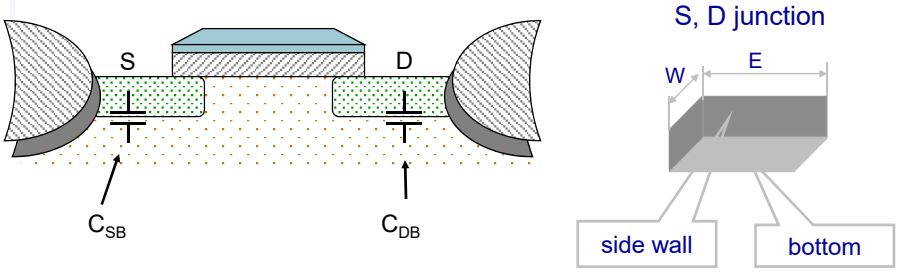


Cut off Saturation Linear

Total gate capacitance change in different operation region.

Junction Capacitance

- C_{SB} and C_{DB} are capacitances between the sidewalls and the bottom regions of the S and D junctions.



Parasitic Capacitances

- Since source – drain doping profiles are normally the same. We take drain capacitance as an example.
- For certain bias voltage V_{BD} the drain-bulk capacitance is:

$$C_{DB} = \frac{C_{DB0}}{\left(1 - \frac{V_{BD}}{P_B}\right)^{M_J}}$$

  - M_J Bulk junction sidewall capacitance grading coefficient
  - P_B Bulk junction built-in potential
- Zero bias drain capacitance C_{DB0} is:

$$C_{DB0} = C_{bottom0} + C_{sidewall0} = A_D C_J + (W + 2E) C_{JSW}$$

  - C_J Zero bias bulk junction bottom capacitance per unit area
  - C_{JSW} Zero bias bulk junction sidewall capacitance per meter of junction perimeter
  - E Drain width
  - A_D Drain area from the layout

Parasitic Resistances

- R_S and R_D are the source and drain resistances due to which inside source and drain voltages applied to actual inversion layer will change for high drain current.
- In addition, there are noise coefficients which may add some noise to I_D.
- This model ignores many parasitic resistances, bipolar devices and PNPN devices.

Lumped Small Signal (AC) Model

- The complete representation for NMOS and PMOS devices is captured in the following figures.
- All capacitors are lumped together.
- For analytic calculations, this simple model is adequate. Computer simulation tools like SPICE use more sophisticated models that including hundreds of parameters.
- For low frequency analysis of the circuits, all capacitors can be removed from the small signal model of the transistor.
- For full AC analysis, all elements are included in the small signal model.
- C_{GB} and C_{GD} can be removed as they are very small compared to others in saturation region.

Lumped Small Signal (AC) Model