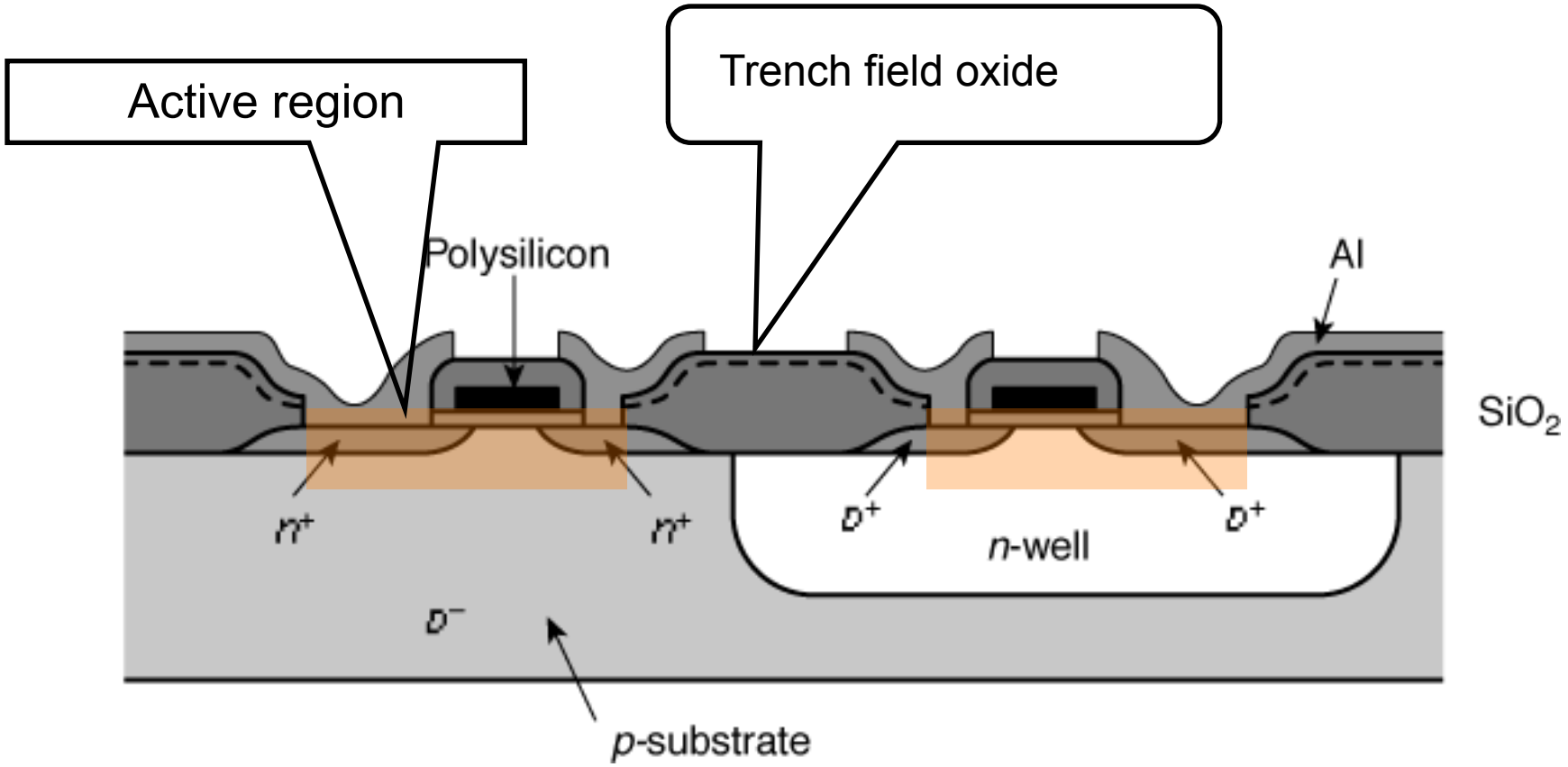
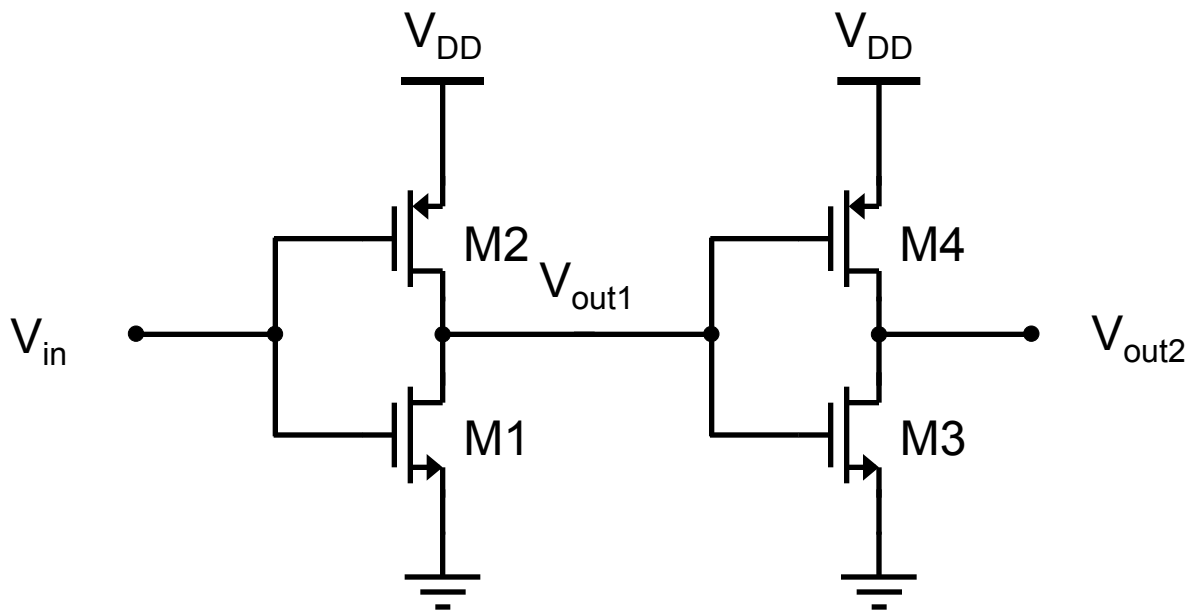
Lecture 2

Introduction of Silicon Processing, Layout and Design Rules

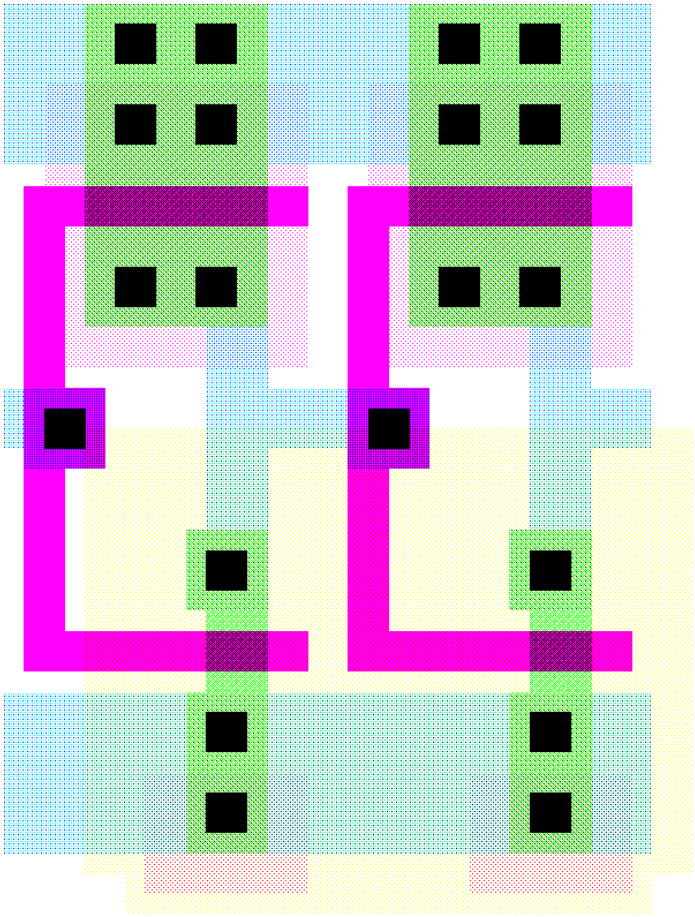
CMOS Process



Circuit View



Layout View



CMOS Process

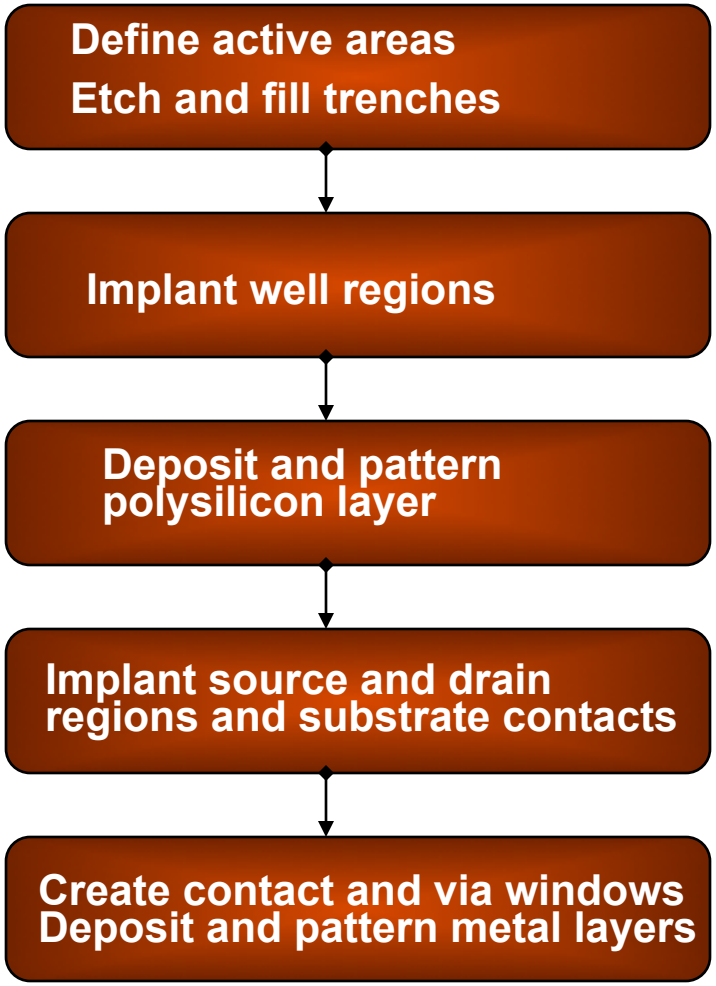
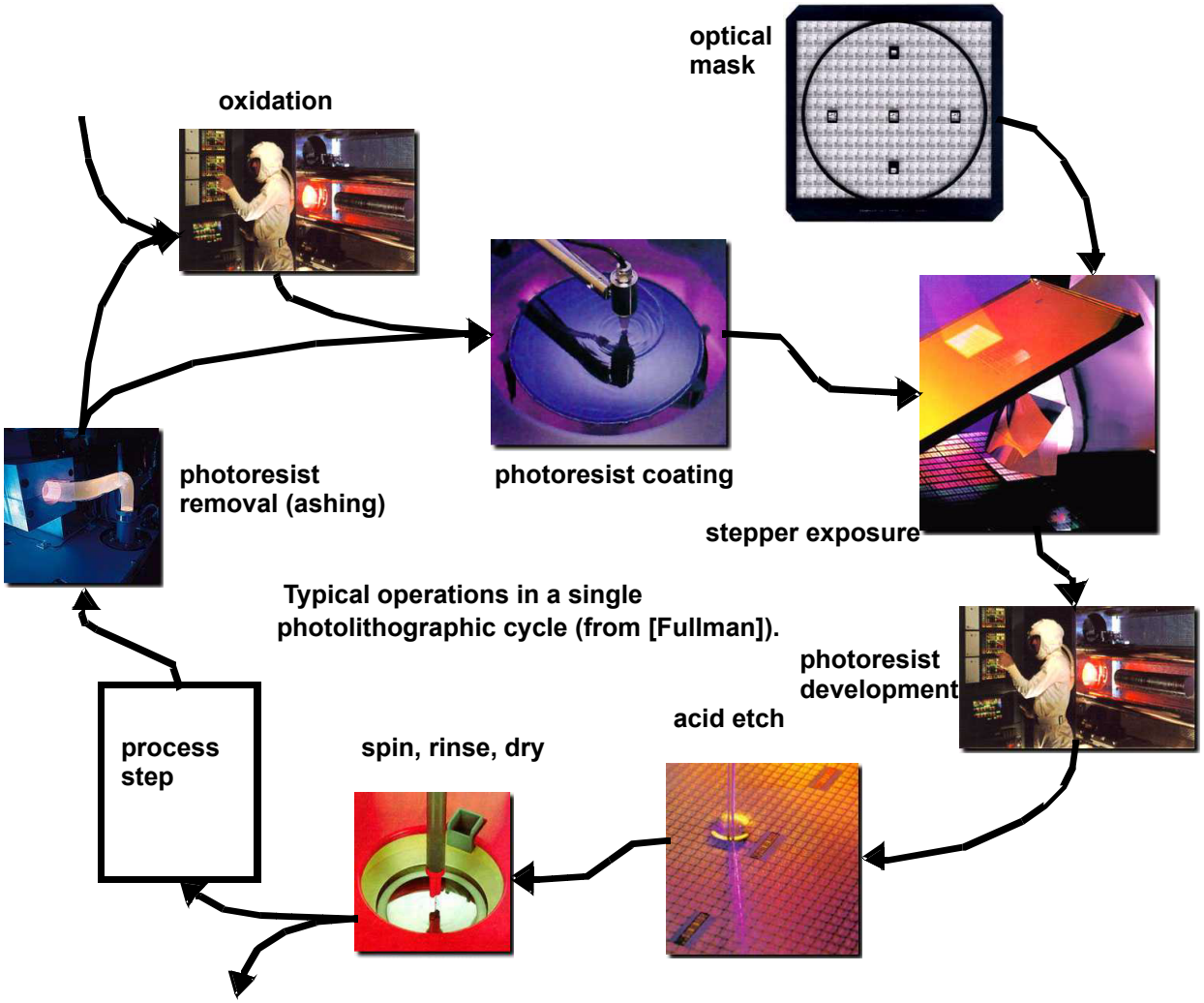
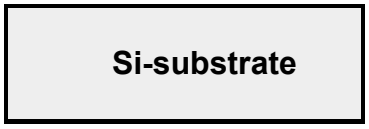


Photo-Lithographic Process

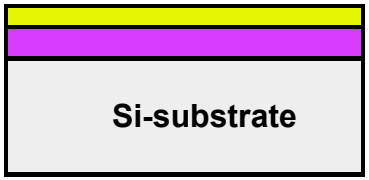


Typical operations in a single photolithographic cycle (from [Fullman]).

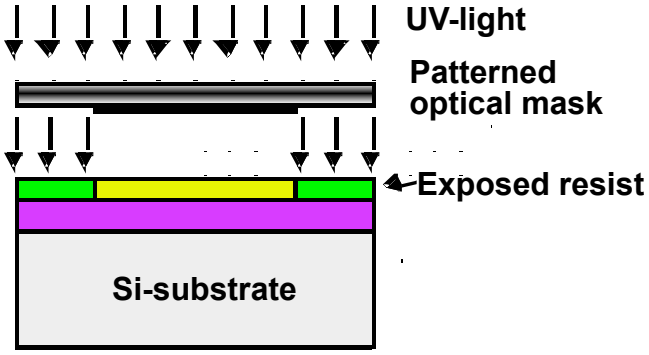
Patterning of SiO2



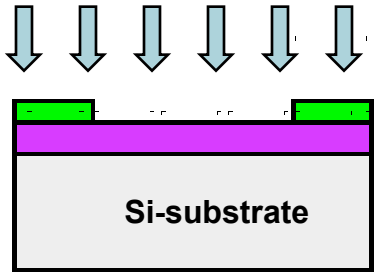
(a) Silicon base material



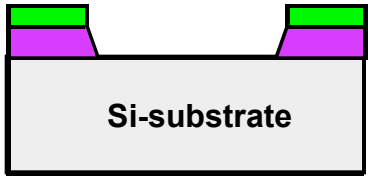
(b) After oxidation and deposition of negative photoresist



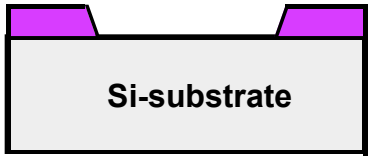
(c) Stepper exposure



(d) After development and etching of resist, chemical or plasma etch of SiO_2

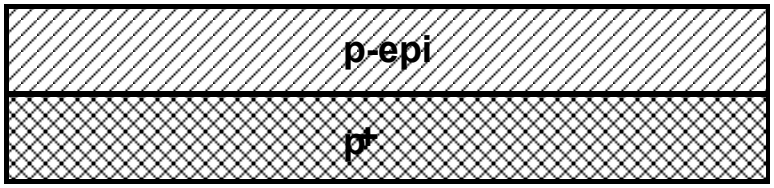


(e) After etching

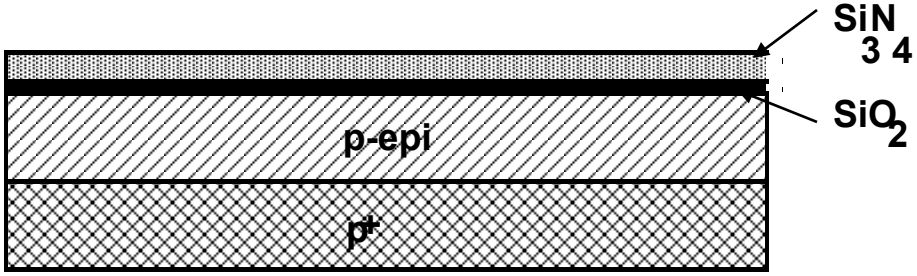


(f) Final result after removal of resist

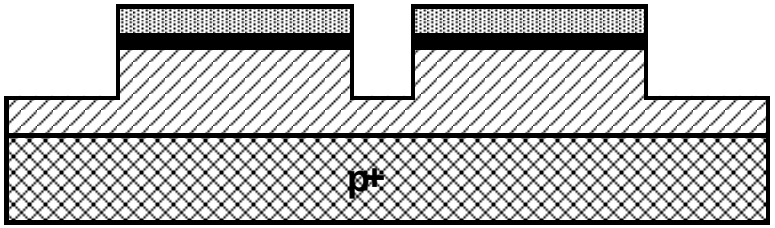
CMOS Process 1



(a) Base material: p+ substrate with p-epi layer

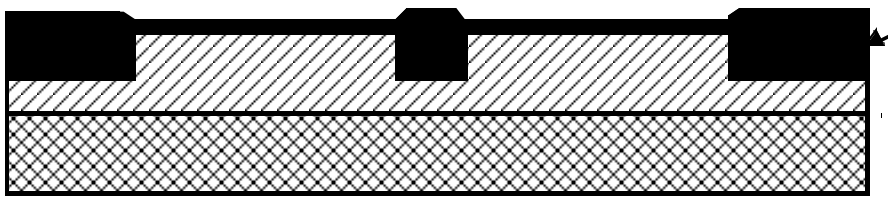


(b) After deposition of gate-oxide and sacrificial nitride (acts as a buffer layer)

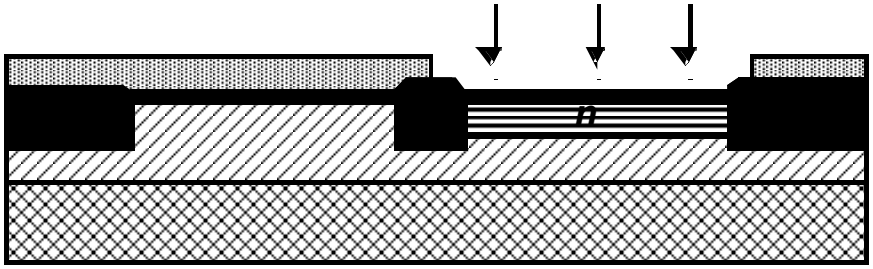


(c) After plasma etch of insulating trenches using the inverse of the active area mask

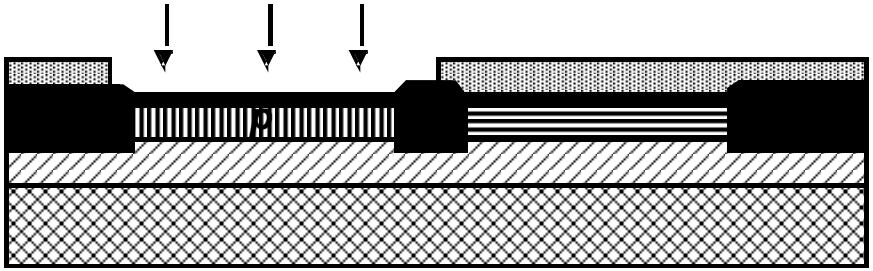
CMOS Process 2



(d) After trench filling, CMP planarization, and removal of sacrificial nitride

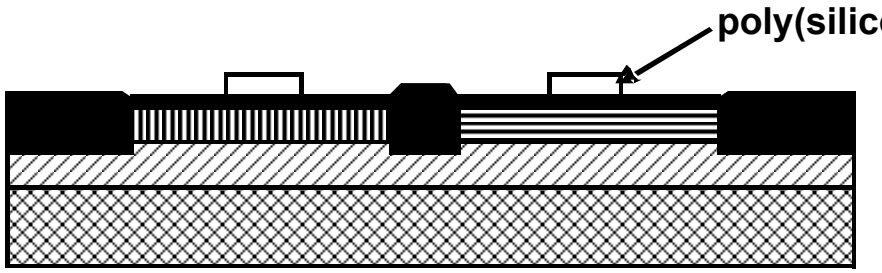


(e) After n-well and V_{Tp} adjust implants

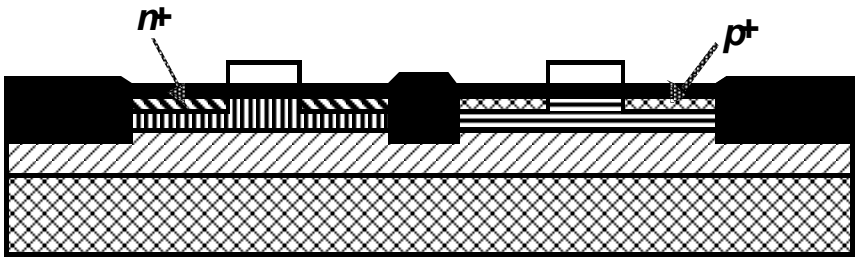


(f) After p-well and V_{Tn} adjust implants

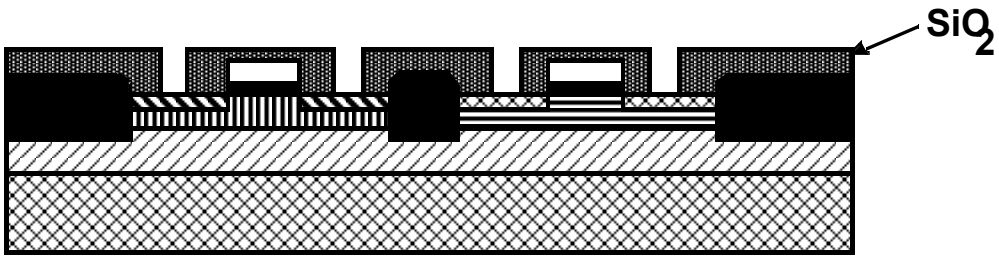
CMOS Process 3



(g) After polysilicon deposition and etch

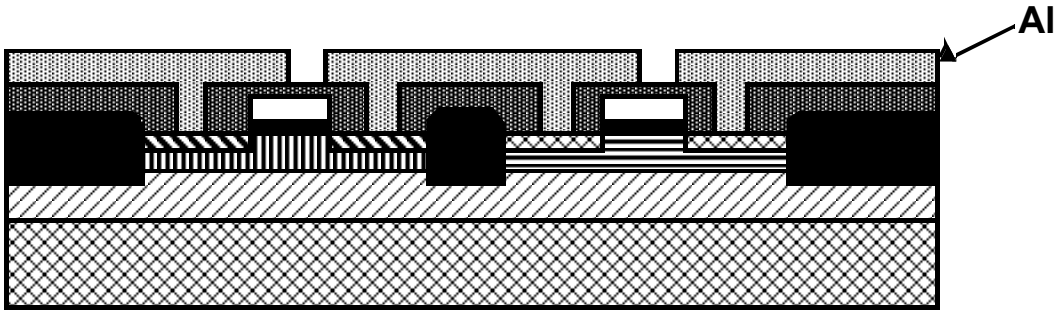


(h) After $n+$ source/drain and $p+$ source/drain implants. These steps also dope the polysilicon.

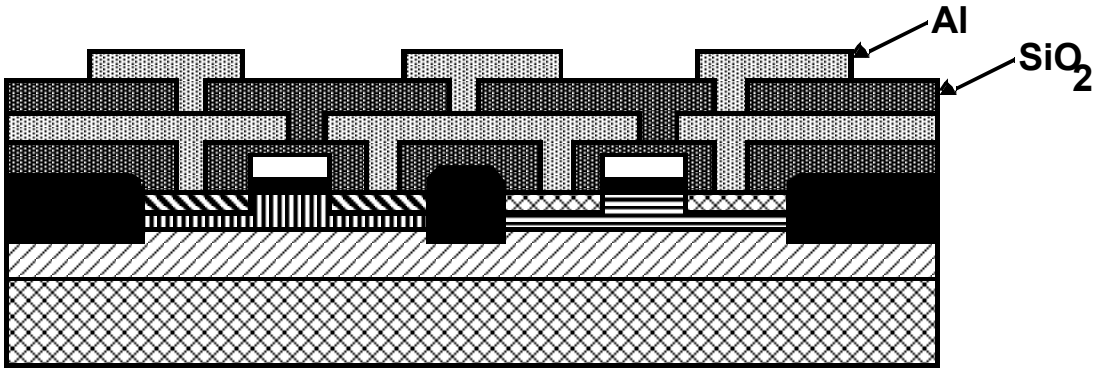


(i) After deposition of SiO_2 insulator and contact hole etch.

CMOS Process 4

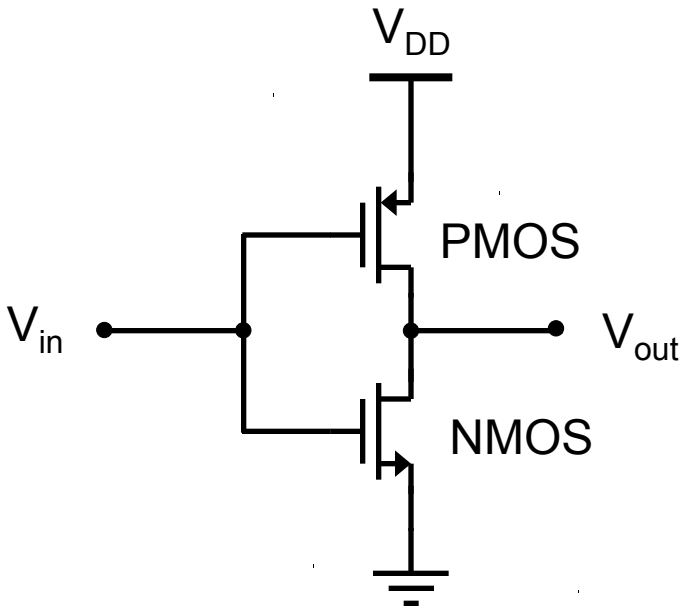


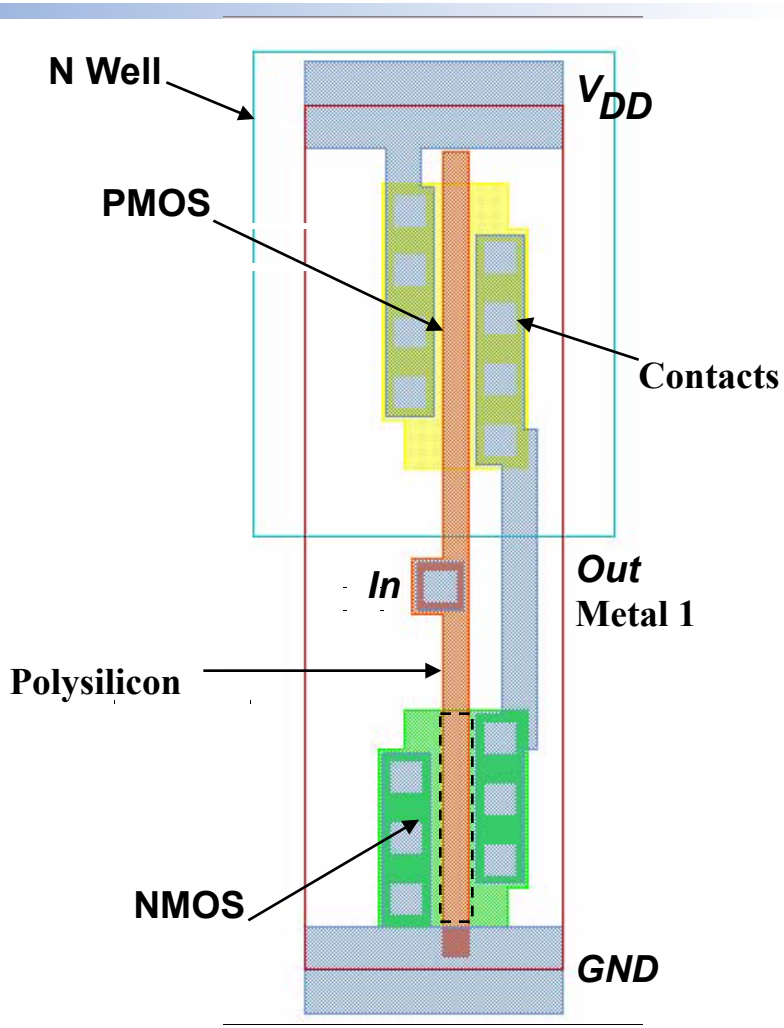
(j) After deposition and patterning of first Al layer.



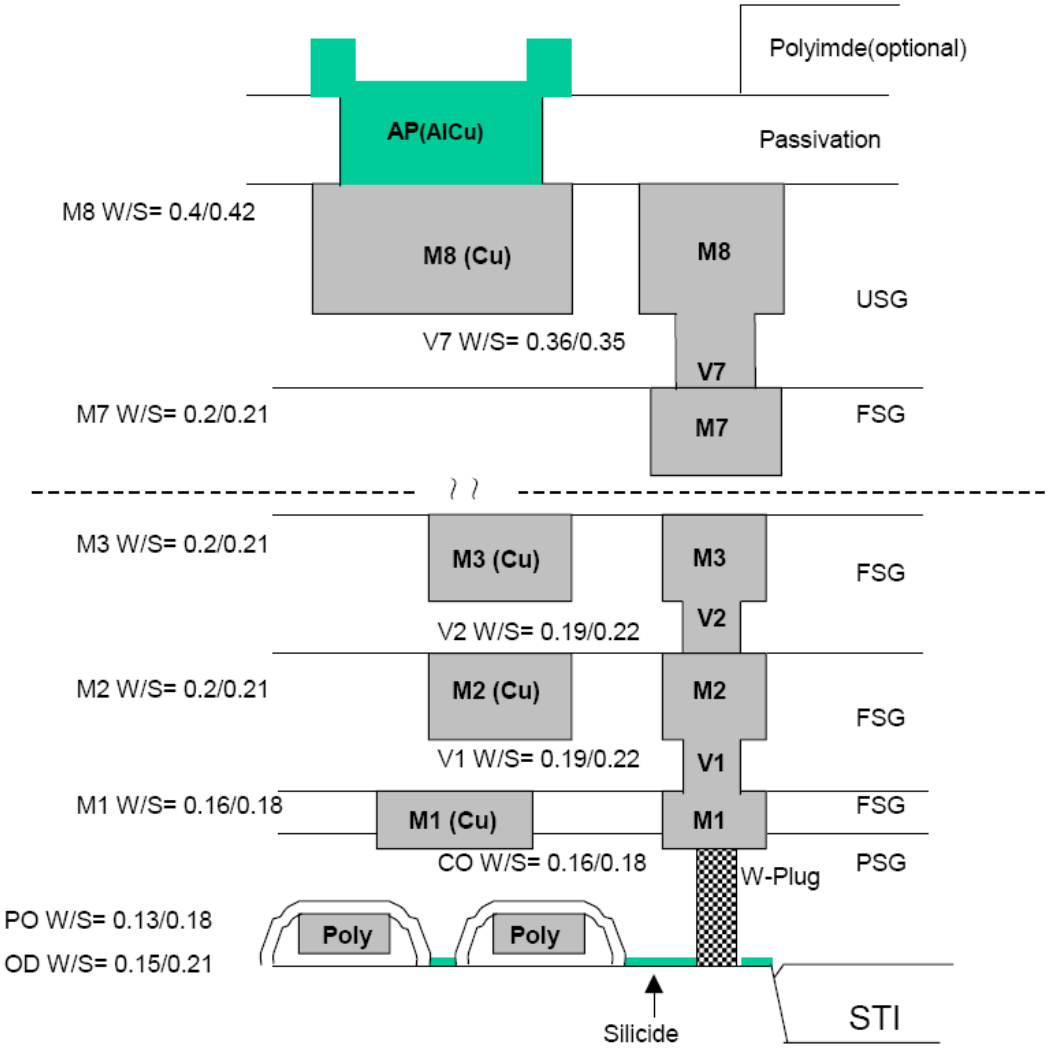
(k) After deposition of SiO_2 insulator, etching of via's, deposition and patterning of second layer of Al.

MOSFET and layout

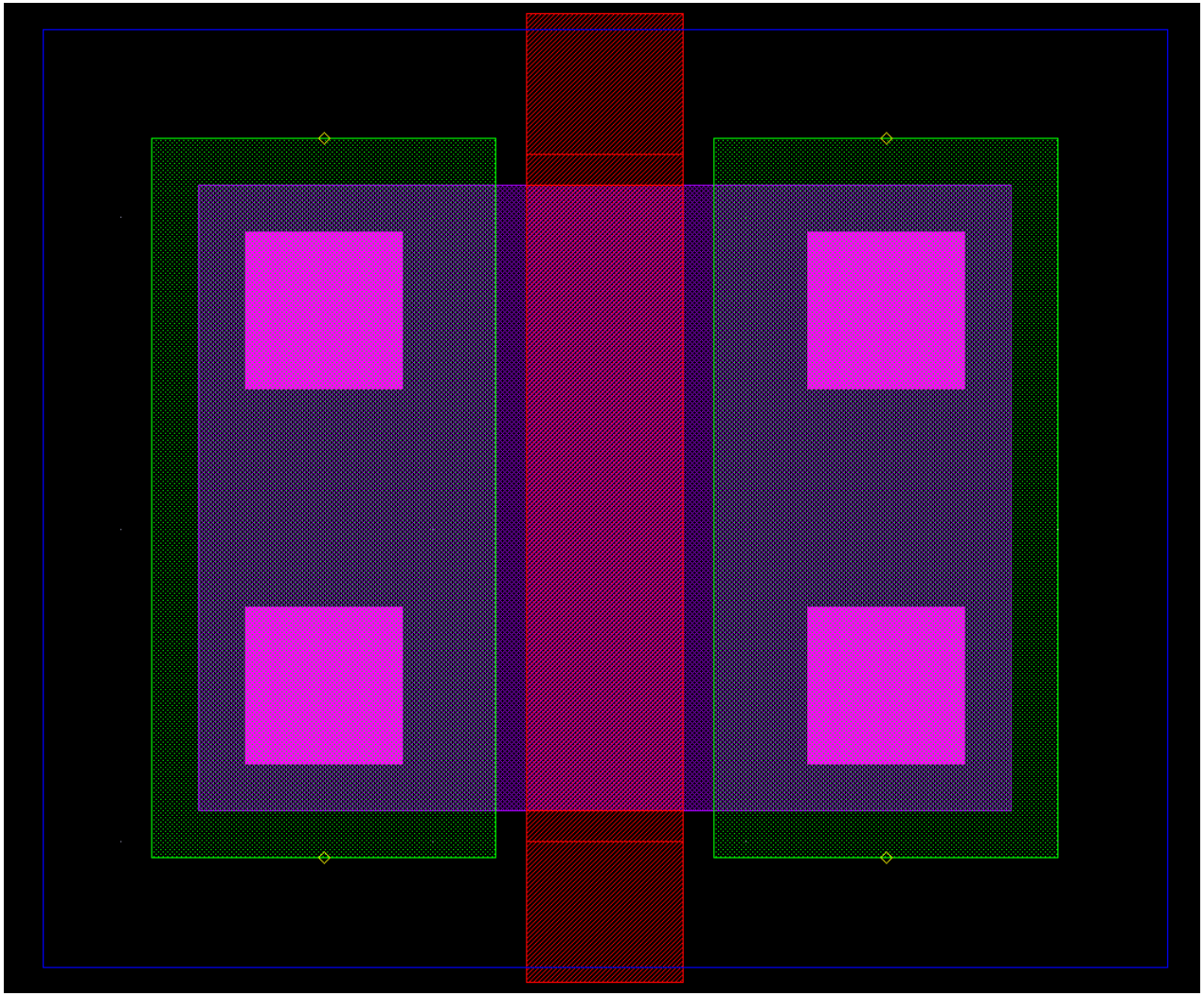




Cross-section of a CMOS Process

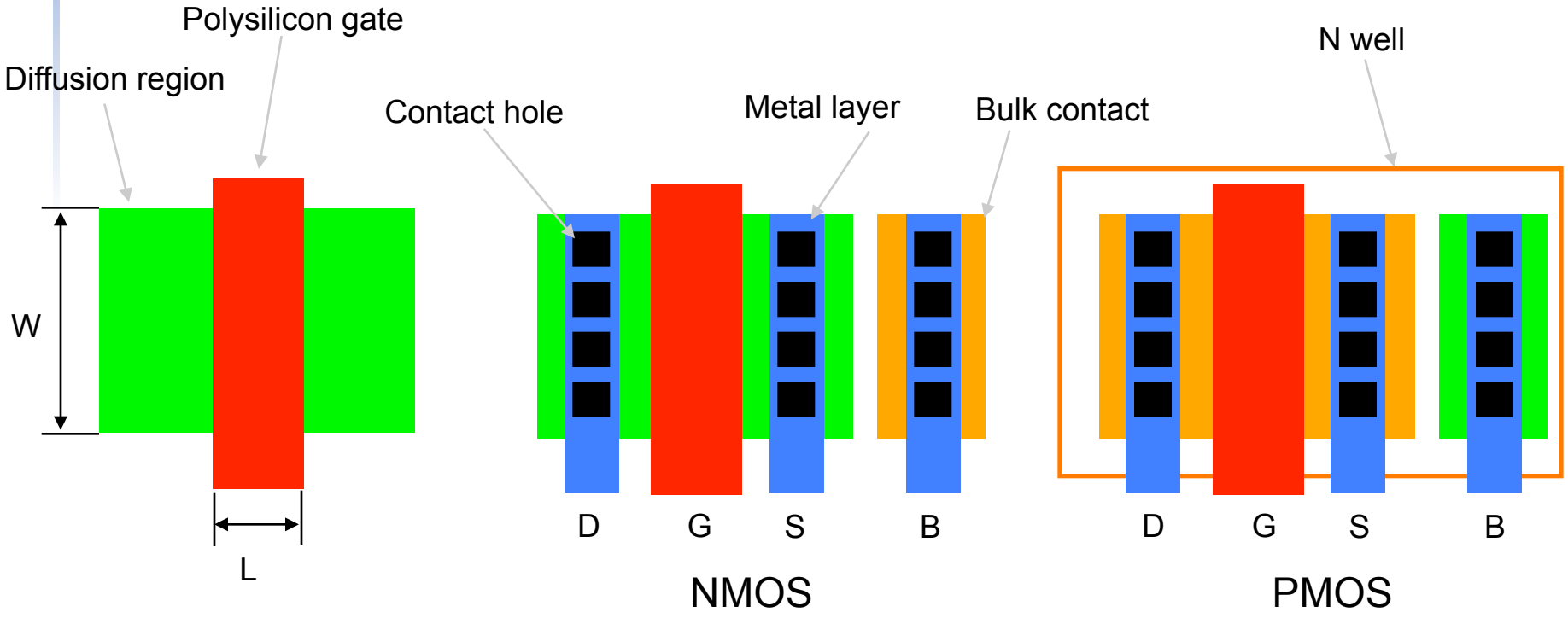


Transistor Layout

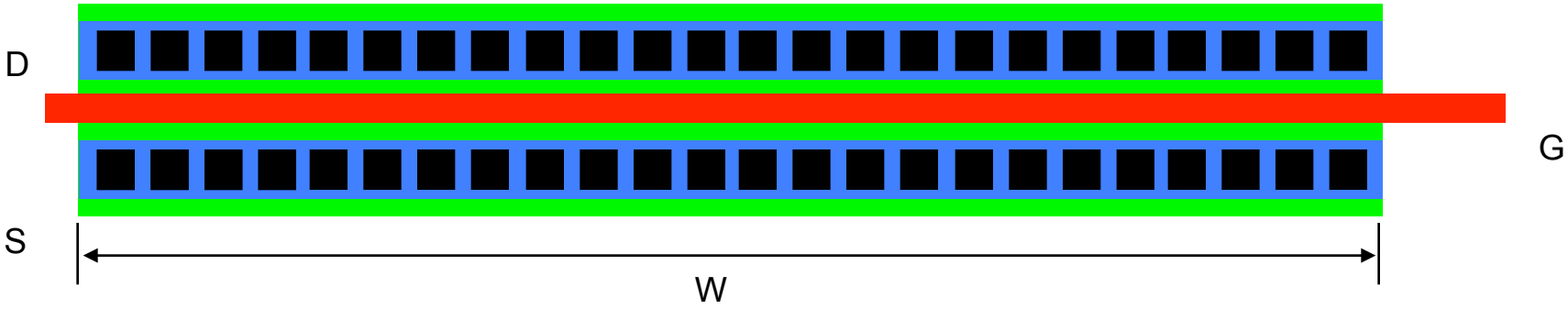


Transistor Layout

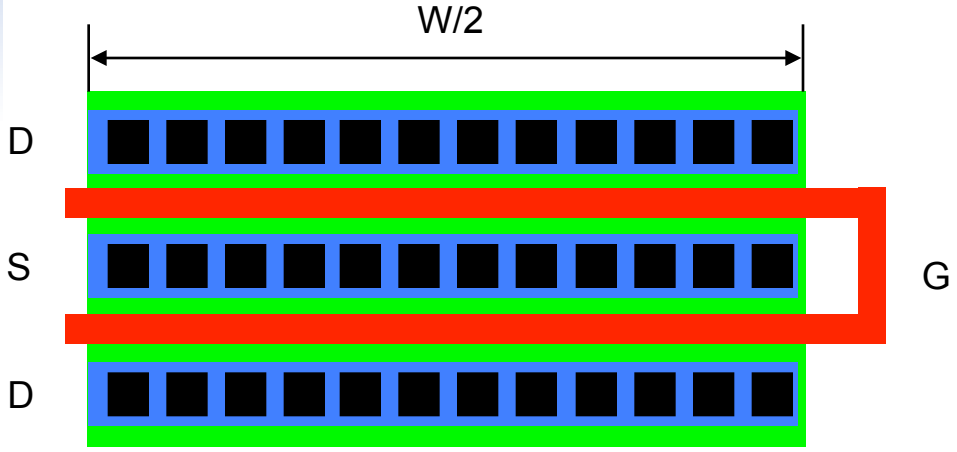
- A MOS transistor is simply a cross of two rectangles: active (diffusion) region and polysilicon gate.
- Make source and drain connection.
- Make substrate (well) contacts.



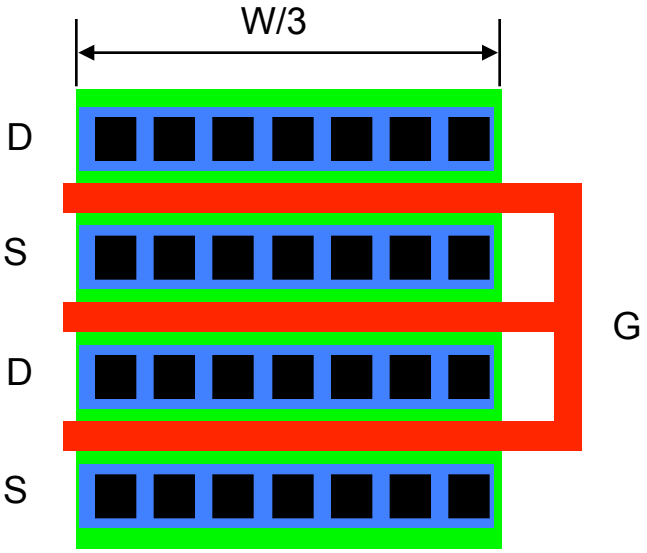
Multi Finger Transistor



C_{SB1} C_{DB1}



C_{SB} =1/2C_{SB1}, C_{DB}=C_{DB1}



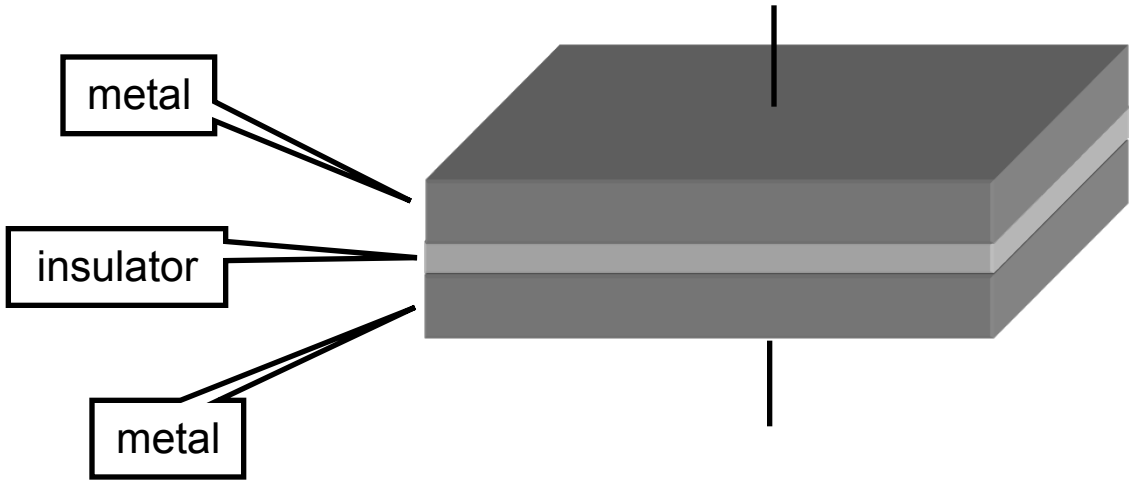
C_{SB} =2/3C_{SB1}, C_{DB}=2/3C_{DB1}

Passive Devices in CMOS

- Passive devices, i.e. resistors, capacitors and inductors, are essential component in analog circuits.
- For analog IC, passive device occupies larger silicon area than MOSFET does.
- Only small-value capacitor and inductor are available in CMOS process.
- Try to avoid passive devices in analog IC.
  - Use transistor in linear region to replace the resistor.
  - Use gate capacitance to replace the capacitor.

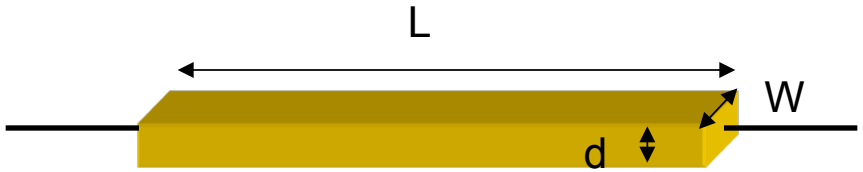
Passive Devices Implementation

- For small value capacitors, we can use MIM (metal insulator metal) capacitor or PIP (poly insulator poly) capacitor.
- MIM cap is not a standard CMOS process step → needs additional masks and process steps.
- Small unit capacitance → usually around 1fF/μm^2.
- Larger process variation -- ±20%.



Passive Devices Implementation

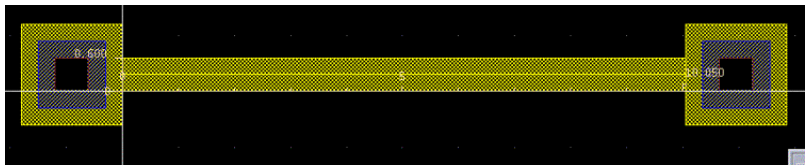
- For resistor, we can use poly resistor (sheet resistance ~100-1000 Ω/square).
- Low resistivity → larger area for high resistance value resistor.
- Larger process variation -- ±20%.
- Parasitic capacitance to substrate.



$$R = \frac{L}{Wd}\rho$$

$$R_0 = \frac{\rho}{d}$$

Sheet resistance



Design Rules

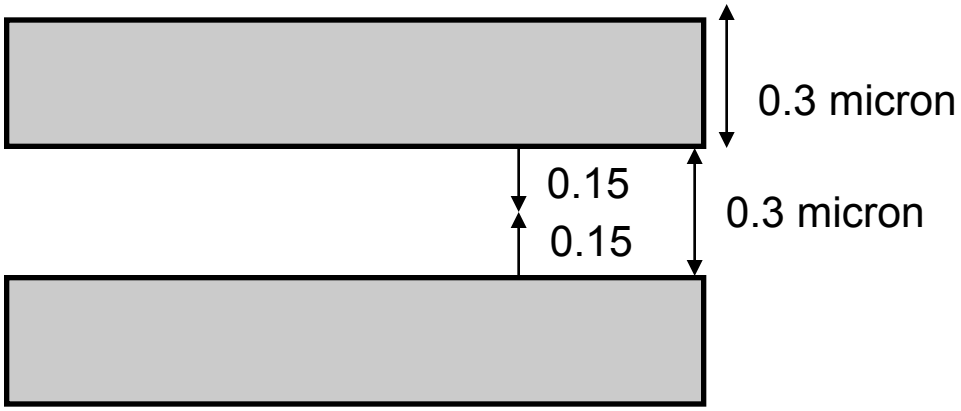
- Interface between the circuit designer and process engineer.
- Guidelines for constructing process masks.
- Unit dimension: minimum line width
  - scalable design rules: lambda parameter
  - absolute dimensions: micron rules
- Rules constructed to ensure that design works even when small fabrication errors (within some tolerance) occur.
- A complete set includes:
  - set of layers
  - intra-layer: relations between objects in the same layer
  - inter-layer: relations between objects on different layers

Layers in a Process

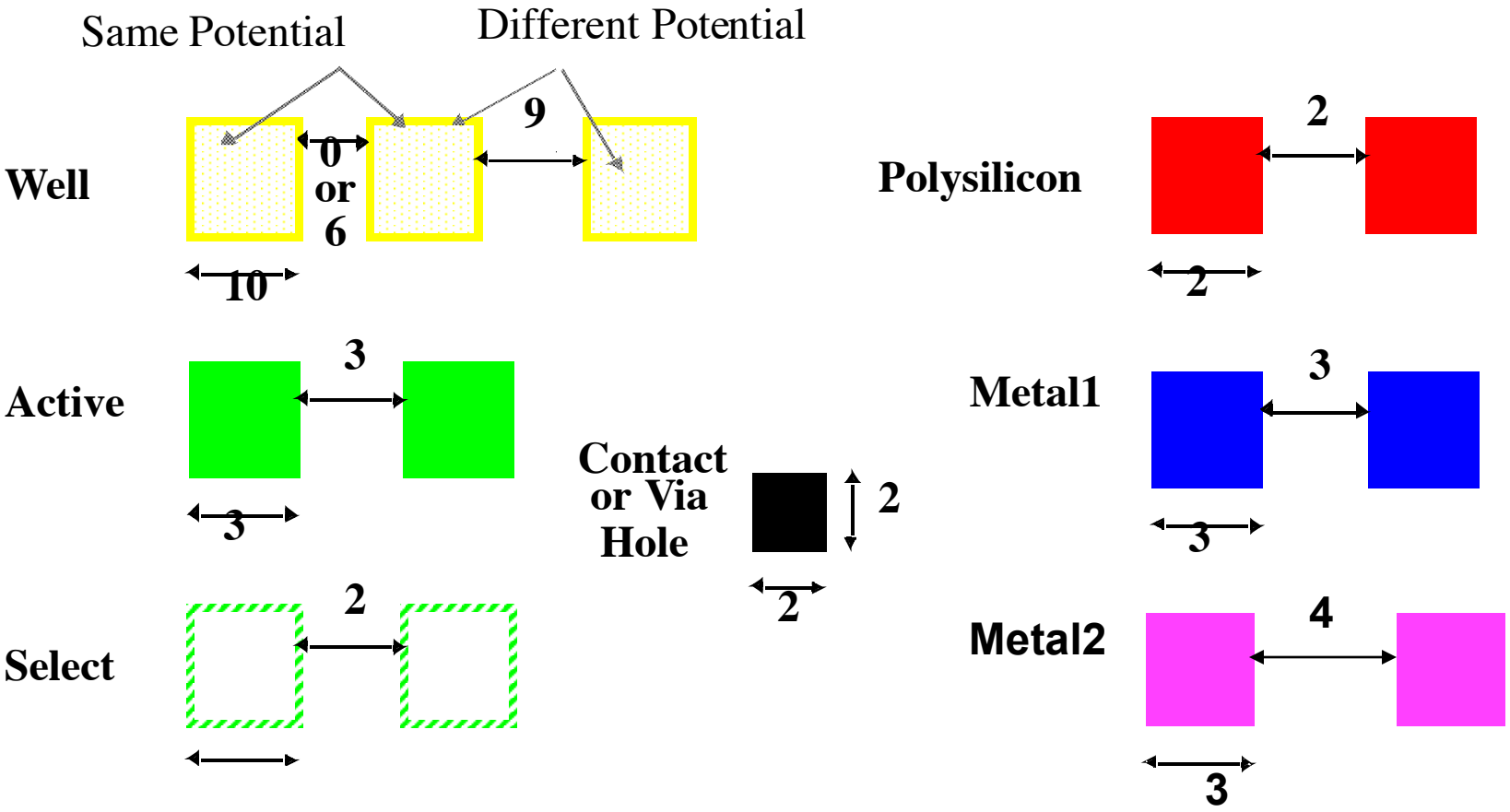
Layer	Color	Representation
Well (p,n)	Yellow	
Active Area (n+,p+)	Green	
Select (p+,n+)	Green	
Polysilicon	Red	
Metal1	Blue	
Metal2	Magenta	
Contact To Poly	Black	
Contact To Diffusion	Black	
Via	Black	

Intra-Layer Rules

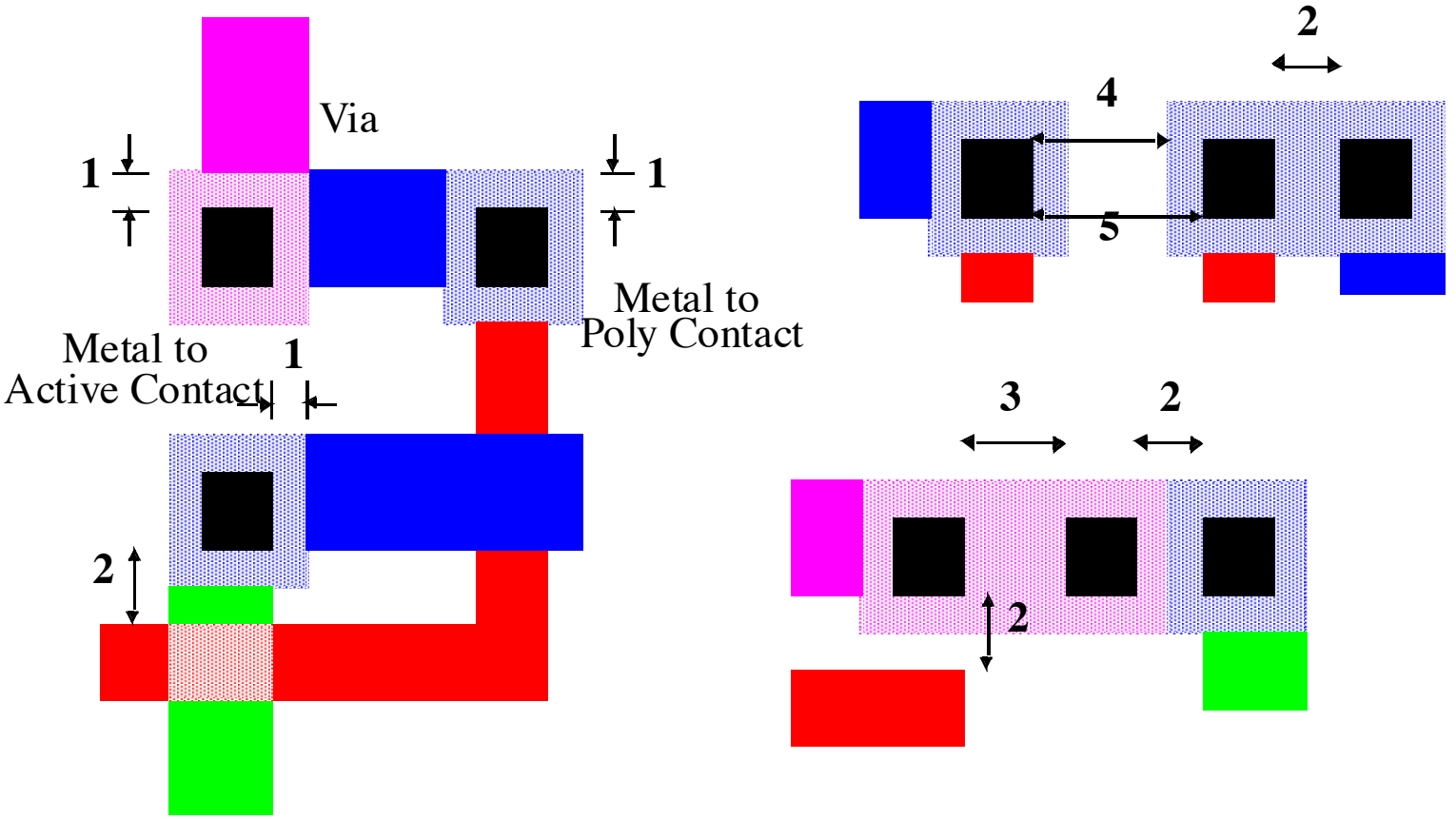
- Minimum dimensions (e.g., widths) of objects on each layer to maintain that object after fabrication.
  - minimum line width is set by the resolution of the patterning process (photolithography).
- Minimum spaces between objects (that are *not* related) on the same layer to ensure they will not short after fabrication.



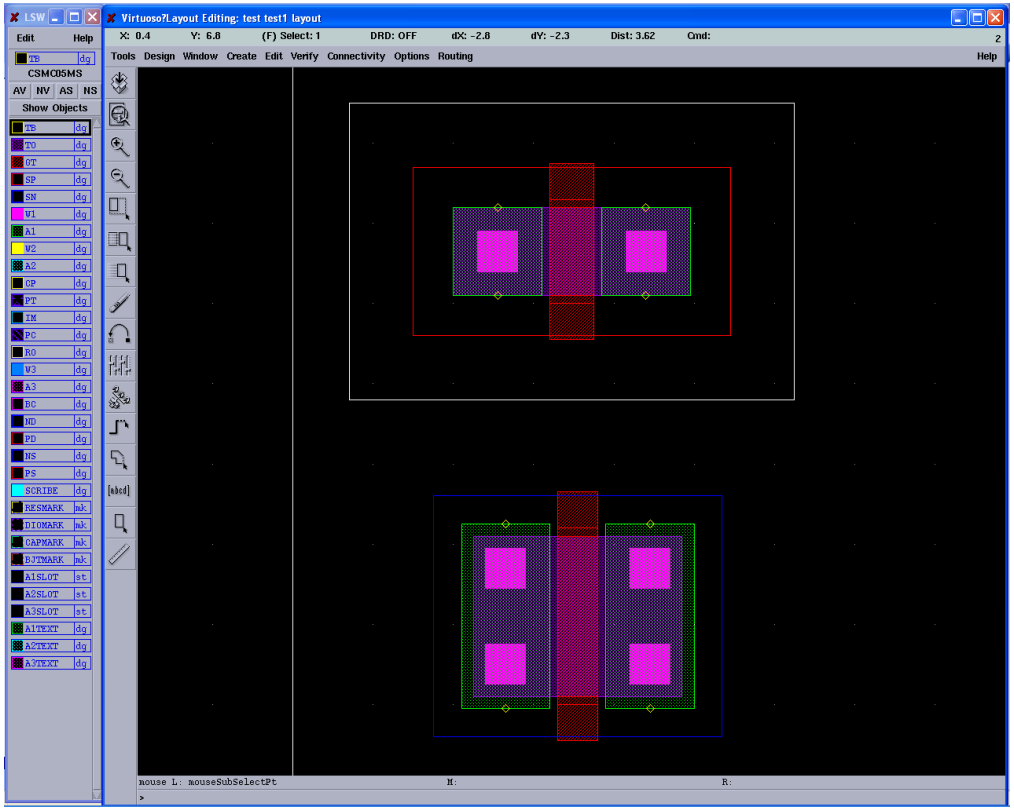
Intra-Layer Design Rules



Inter-Layer Design Rules

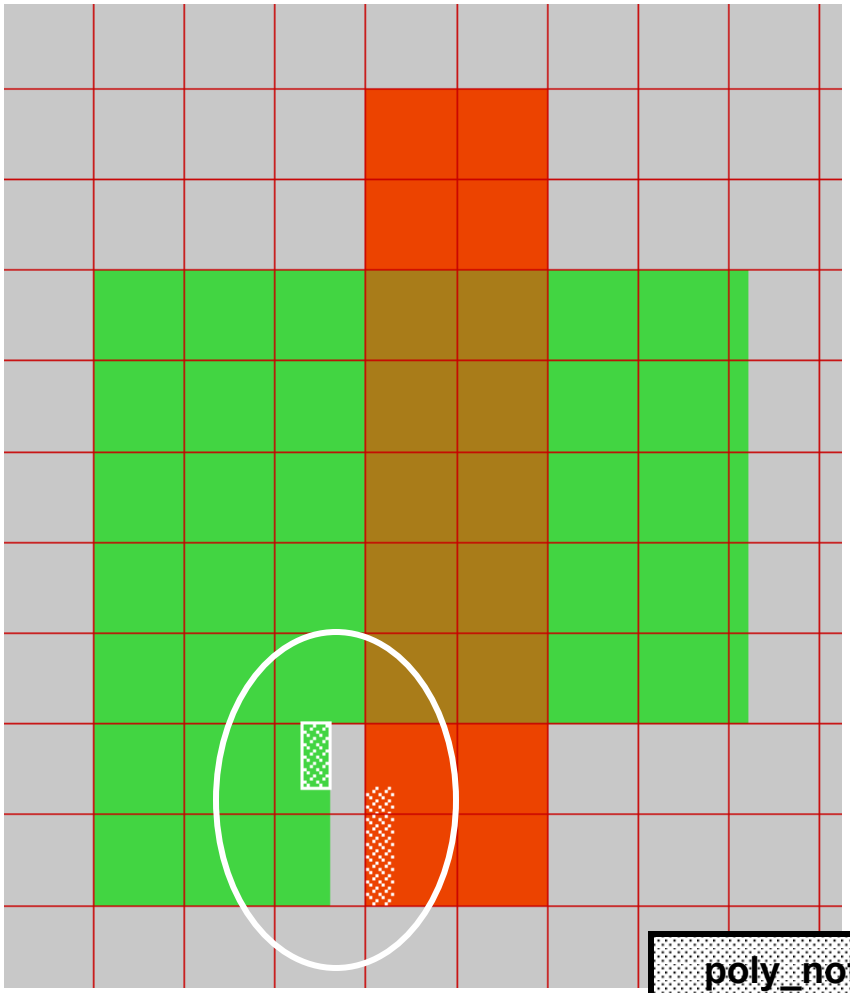


Layout Editor-Cadence Virtuoso



- Layout editor is the layout tools helps to generate the mask patterns.
- It uses different colors and patterns to represent different layers in the mask.
- The output data is normally in GDSII format, which is the final result of the design.

Design Rule Check



- Analog design is not fully automated → errors are inevitable.
- Design rule check (DRC) checks whether the layout violates any design rules.
- DRC can give you feedback on the violations.
- Re-draw the layout and re-do the DRC until no DRC errors reported.

poly_not_fet to all_diff minimum spacing = 0.14 um.

Layout vs. Schematic Check

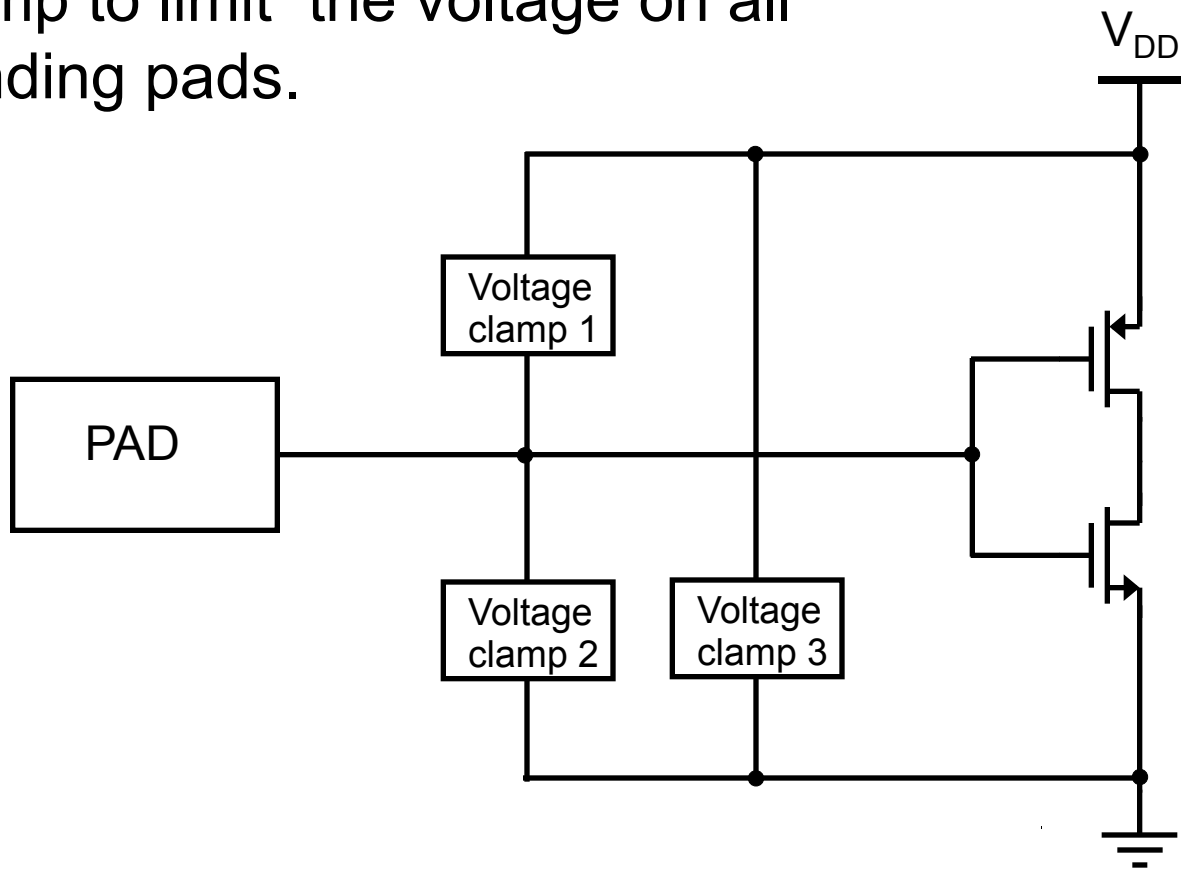
- Layout vs. Schematic Check (LVS) checks whether the layout corresponds with the schematic.
- LVS compares the netlist generated from the schematic with the netlist generated from the layout patterns and gives the comparison result.
- LVS checks the electrical connections as well as the device parameters.
- Design must be DRC and LVS clean → no DRC and LVS errors.
- Tape-out—send the GDSII data to fabrication.

ESD Protection

- ESD stands for Electrostatic Discharge. It is the electrical static charge transfer between two objects with different potentials.
- The ESD can cause large current and destroy semiconductor devices.
- MOSFET gates are very high impedance nodes→ sensitive to ESD.
- To prevent the ESD damaging the devices, a circuit called ESD protection circuit is added inside the IC.

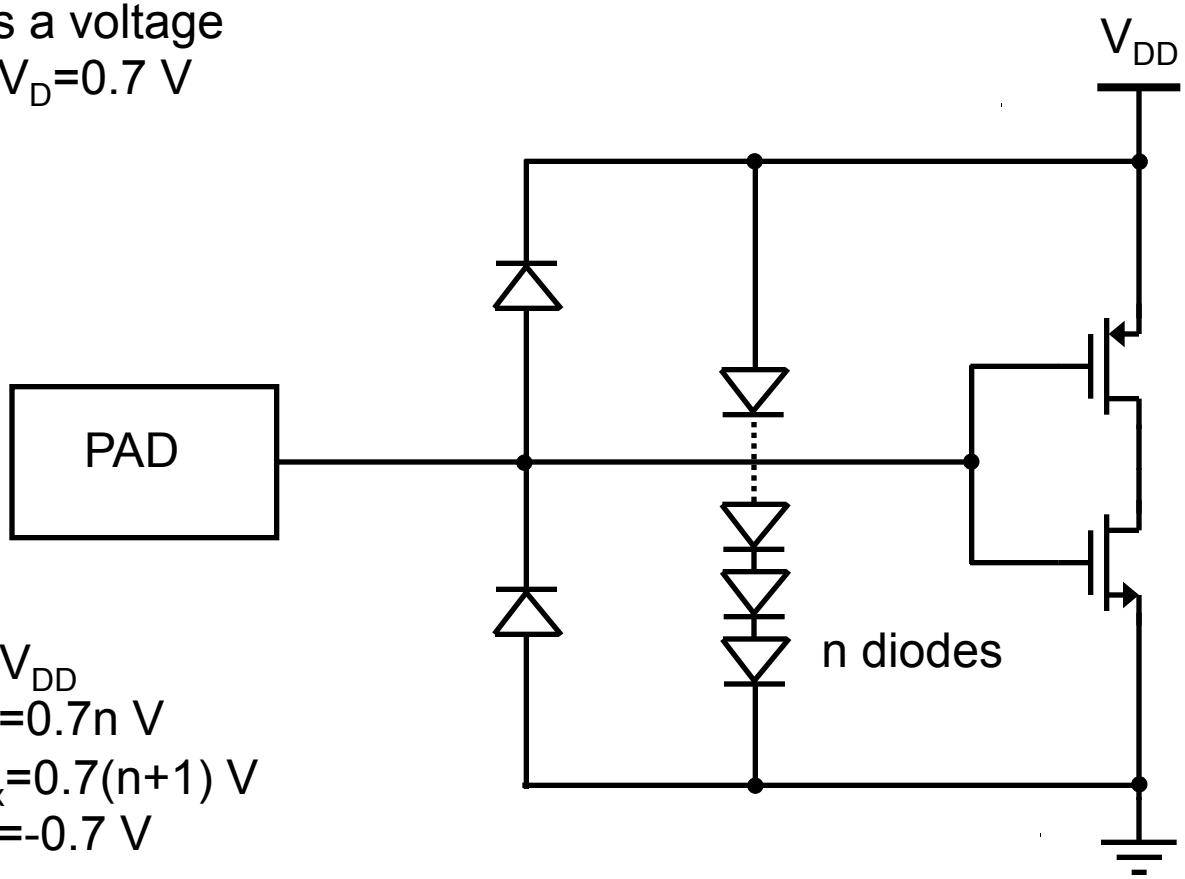
ESD Protection Circuit

- The basic idea is using the voltage clamp to limit the voltage on all bonding pads.



ESD Protection Using Diodes

Diode is a voltage clamp. V_D=0.7 V



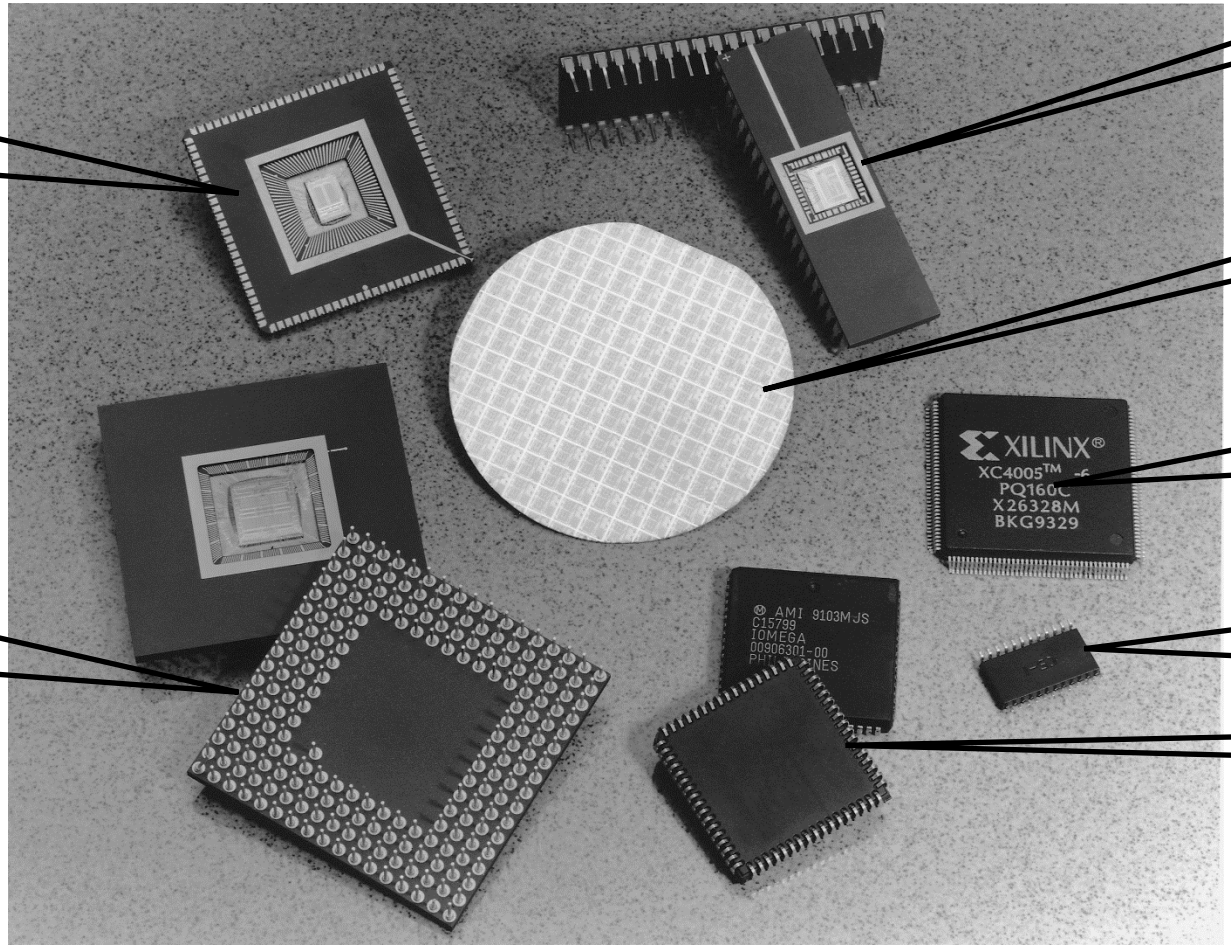
$n*0.7>V_{DD}$

V_{DDmax}=0.7n V

V_{padmax}=0.7(n+1) V

V_{padmin}=-0.7 V

Packaging



Leadless carrier

DIP

Die

Quad plat pack

Pin grid array

Small outlet IC

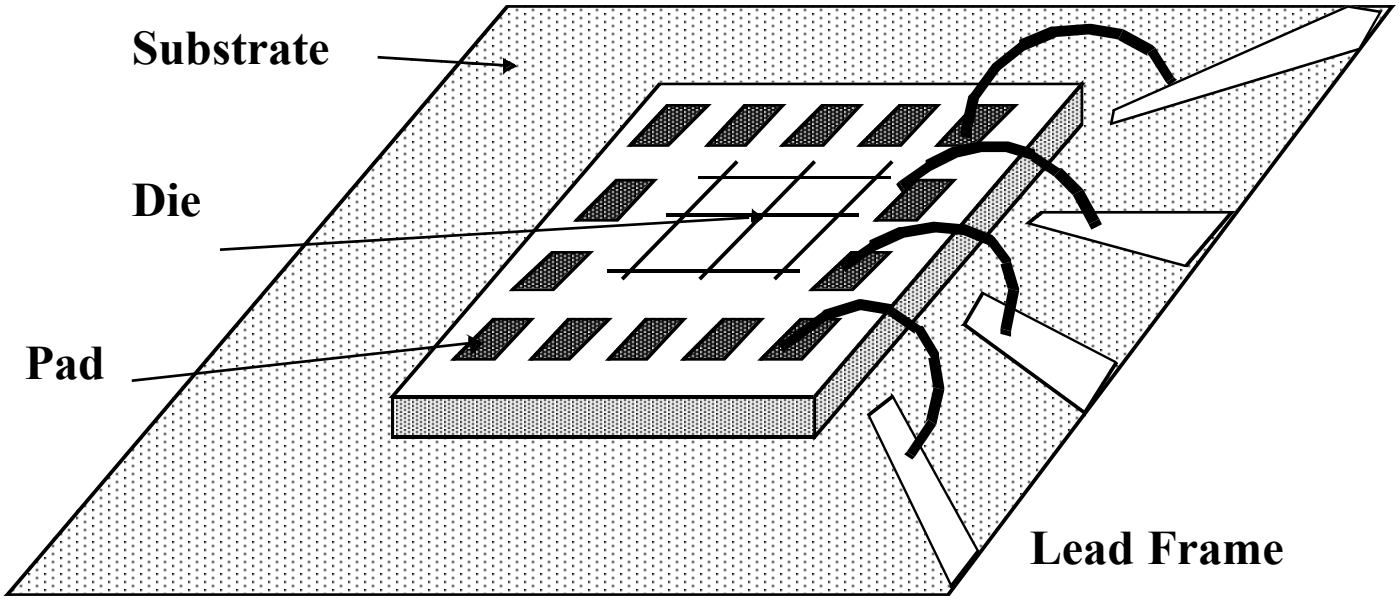
PLCC

Packaging Requirements

- Electrical: Low parasitics
- Mechanical: Reliable and robust
- Thermal: Efficient heat removal
- Economical: Cheap

Wire Bonding

Wire Bonding



Flip-Chip Bonding