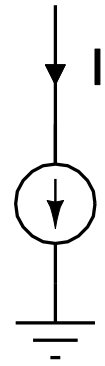
Lecture 3

Current Source and Current Mirror

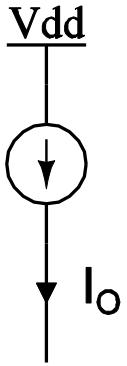
Introduction

- Before any device can be used in any application, it has to be properly biased so that small signal AC parameters are well defined and the device is in proper regime of operation – usually in saturation in analog applications.
- Current mirror method is a simple way to replicate well defined DC current sources in several independent circuit branches and is very popularly used in analog circuit design.
- Current source is also widely used as active load to improve amplifier gain.
- Current mirror is also a basic building block in current domain signal processing circuits.

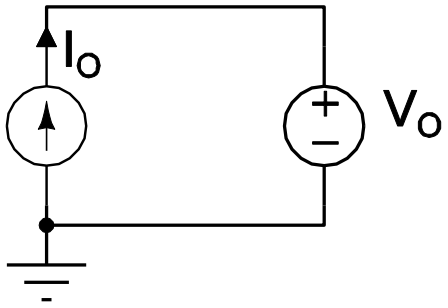
Types of Current Source

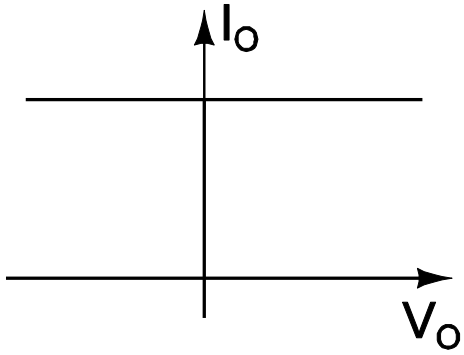


current sink



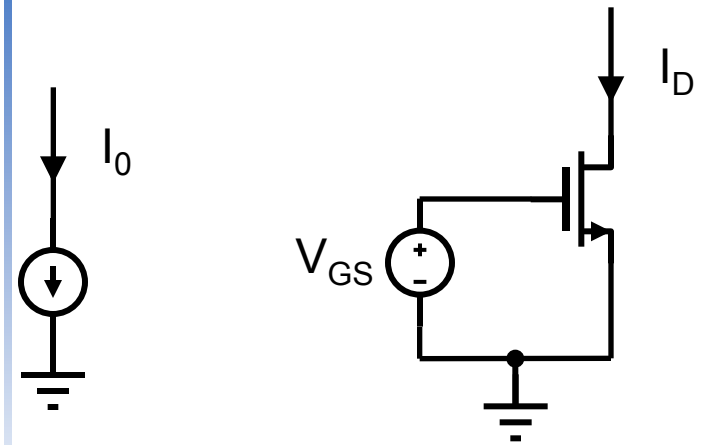
current source

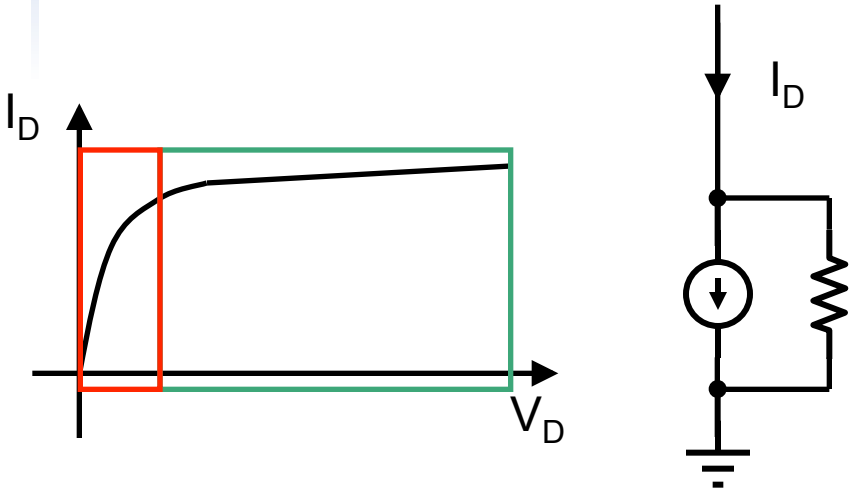




- Current source provides current to external circuit.
- Current sink receives current from the external circuit.
- In this course, we refer both current source and sink as current source.
- I-V plot of an ideal current source is shown.
- Current is not a function of the voltage across the current source.

Realization of Current Source



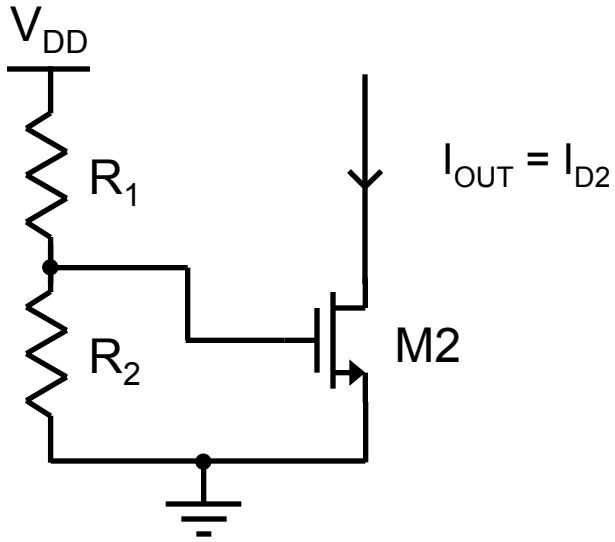


- Realization of current source by MOSFET in saturation region by providing certain V_{GS}.
- I_D is a function of V_{GS}.
- Due to the channel length modulation effect of the MOSFET, the output resistance of the current is finite.
- There is a minimum output voltage for the MOSFET current source, V_{DSsat} to keep the transistor in saturation region.

Basic Current Source Realization

- A simple current source circuit uses a MOS transistor biased with a voltage divider.
- This circuit is sensitive to power supply voltage V_{DD} and the threshold voltage V_{TH}.

$$I_{D2} = \frac{1}{2}\left(\frac{W}{L}\right)_2 \mu C_{OX}\left(\frac{V_{DD}R_2}{R_1+R_2} - V_{TH2}\right)^2(1+\lambda V_{DS2})$$



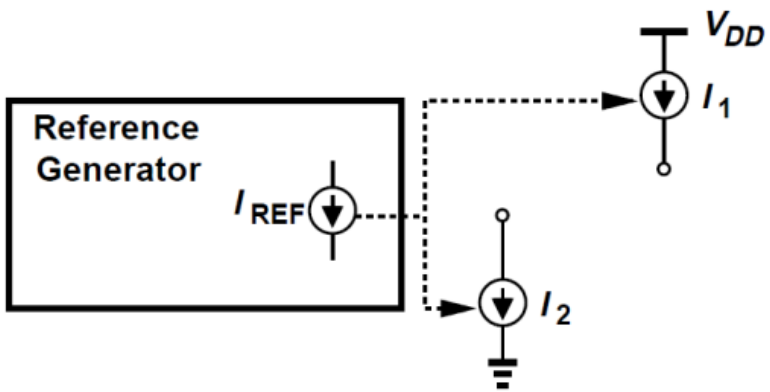
Note: (1) the threshold voltage may vary by 50 to 100 mV from wafer to wafer; (2) both μ_n and V_{TH} exhibit temperature dependence.
A good analog design should be insensitive to Process, supply Voltage and Temperature (PVT) variation.

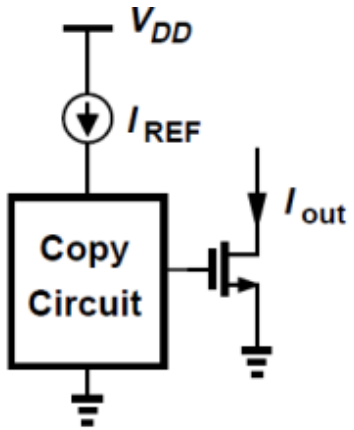
Conceptual Means of Copying Currents

- Use of a reference to generate various currents.

$$I_{out} = f[f^{-1}(I_{REF})] = I_{REF}$$

- Two identical MOS devices that have equal gate-source voltages and operate in saturation carry equal currents

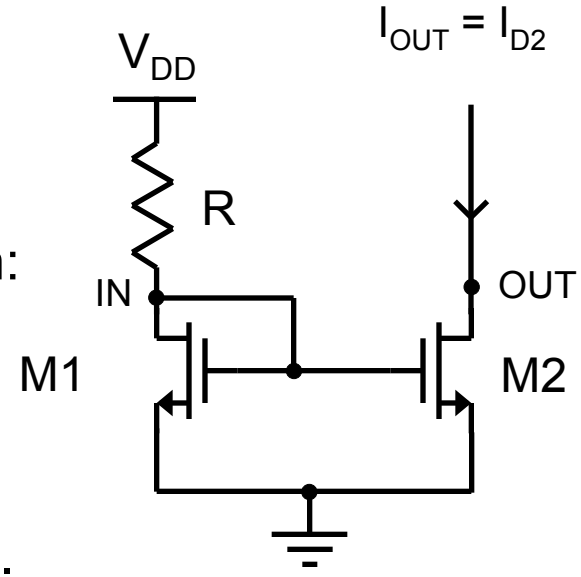




Current Mirror (1)

- Replace R2 with a diode-connected transistor.
- For diode-connected transistor M1, we have:
  $V_{D1} = V_{G1}$, and $V_{TH1}>0$.
  $V_{DS1} = V_{GS1} > V_{GS1} - V_{TH1}$
- Hence, M1 is always in saturation region. Then:

$$I_{D1} = \frac{1}{2}\mu C_{OX}\frac{W}{L}(V_{GS1} - V_{TH1})^2(1+\lambda V_{GS1}) = \frac{V_{DD} - V_{GS1}}{R}$$

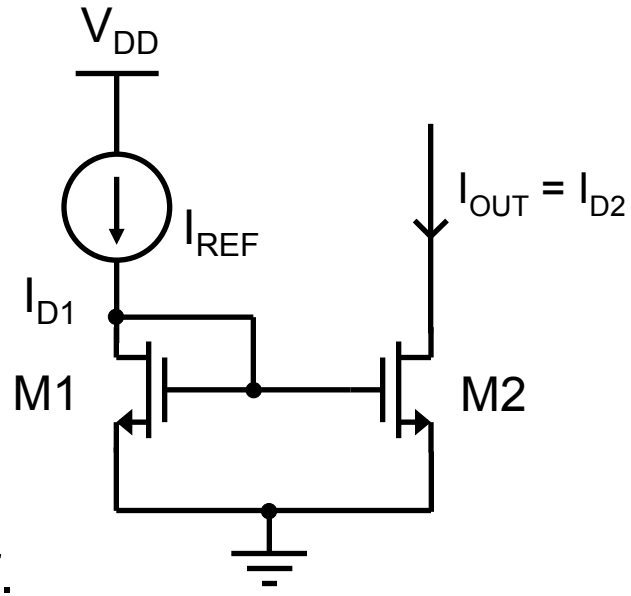


- For given I_{D1}, we can solve the cubic equation to find the gate voltage, and find the value of R.
- If the channel length modulation term is dropped, we can easily calculate the value of R as it is a quadratic equation.

$$I_{D1} = \frac{1}{2}\mu C_{OX}\frac{W}{L}(V_{GS1} - V_{TH1})^2 = \frac{V_{DD} - V_{GS1}}{R}$$

Current Mirror (2)

- More generally, the input current can be replaced with a constant current source I_{REF}. The current mirror copies the current from the reference.
- The basic idea here is to set V_{GS} of M2 to a fixed value by diode connected transistor M1.
- Hence, M2 now looks like a fixed DC current source and should have a very high resistance looking into the drain terminal, presenting characteristic of a typical current source.
- Since both transistors share the same V_{GS}, same process and same temperature variations, the PVT effect will be cancelled off.
- This current source simply utilizes matched devices to cancel PVT effect. This is a usual way in analog circuit designs to deal with PVT.



Current Mirror Analysis

- With accurate model that includes channel length modulation, we have:

$$I_{D1} = \frac{1}{2}\left(\frac{W}{L}\right)_1 \mu C_{OX}(V_{GS1} - V_{TH1})^2(1 + \lambda V_{GS1})$$

$$I_{D2} = \frac{1}{2}\left(\frac{W}{L}\right)_2 \mu C_{OX}(V_{GS1} - V_{TH2})^2(1 + \lambda V_{DS2})$$

- Since both transistors are fabricated with the same process steps, they have the same parameter μC_{OX} and V_{TH}.
- So the current is:

$$\frac{I_{OUT}}{I_{IN}} = \frac{I_{D2}}{I_{D1}} = \frac{\left(W/L\right)_2(1 + \lambda V_{OUT})}{\left(W/L\right)_1(1 + \lambda V_{IN})}$$

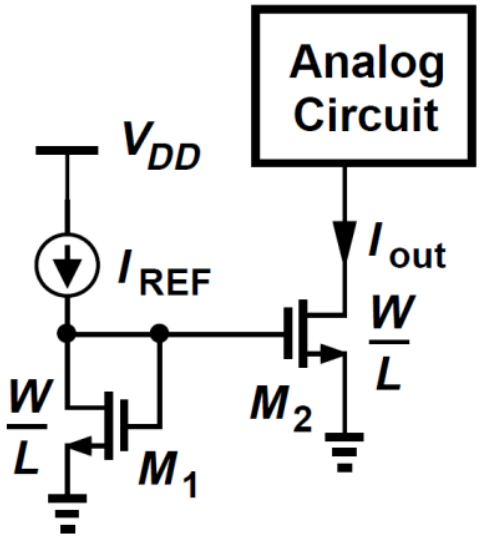
Effect of Channel-Length Modulation

- Neglecting channel-length modulation, we can write

$$I_{REF} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS} - V_{TH})^2$$

$$I_{out} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS} - V_{TH})^2,$$

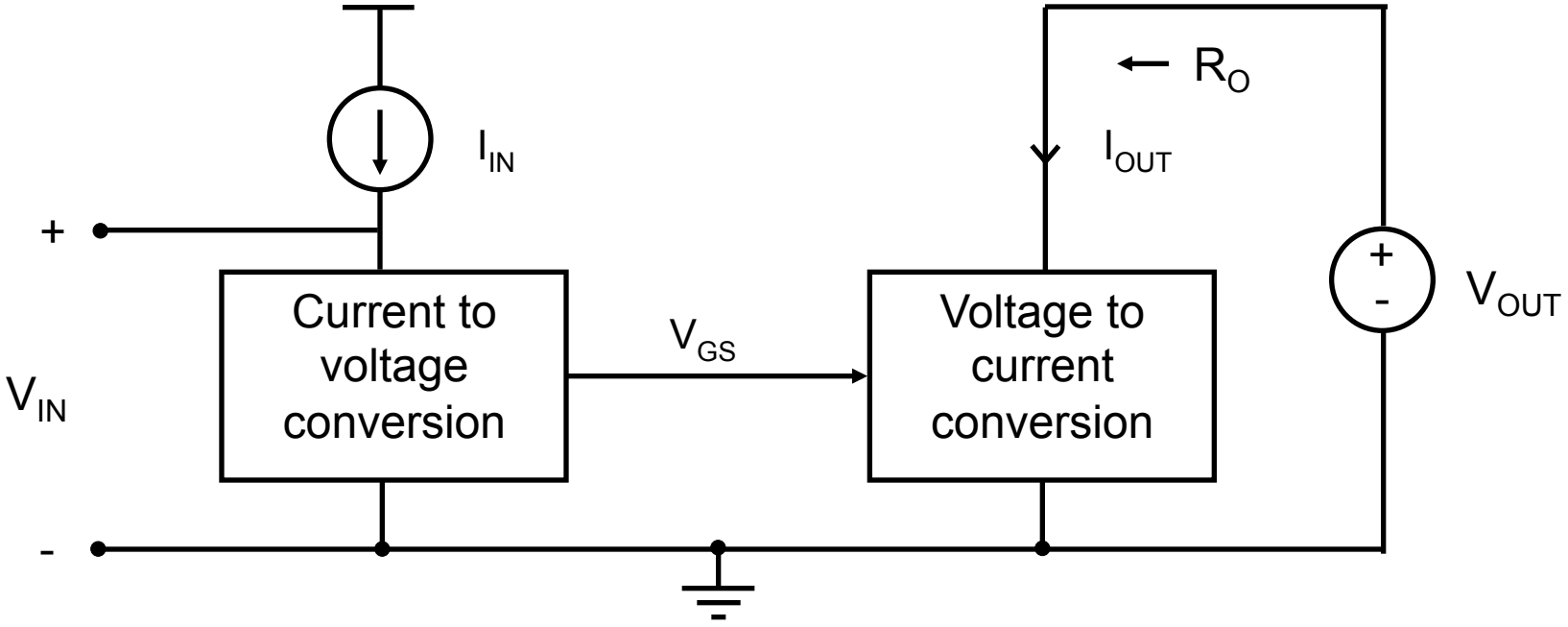
$$I_{out} = \frac{(W/L)_2}{(W/L)_1} I_{REF}.$$



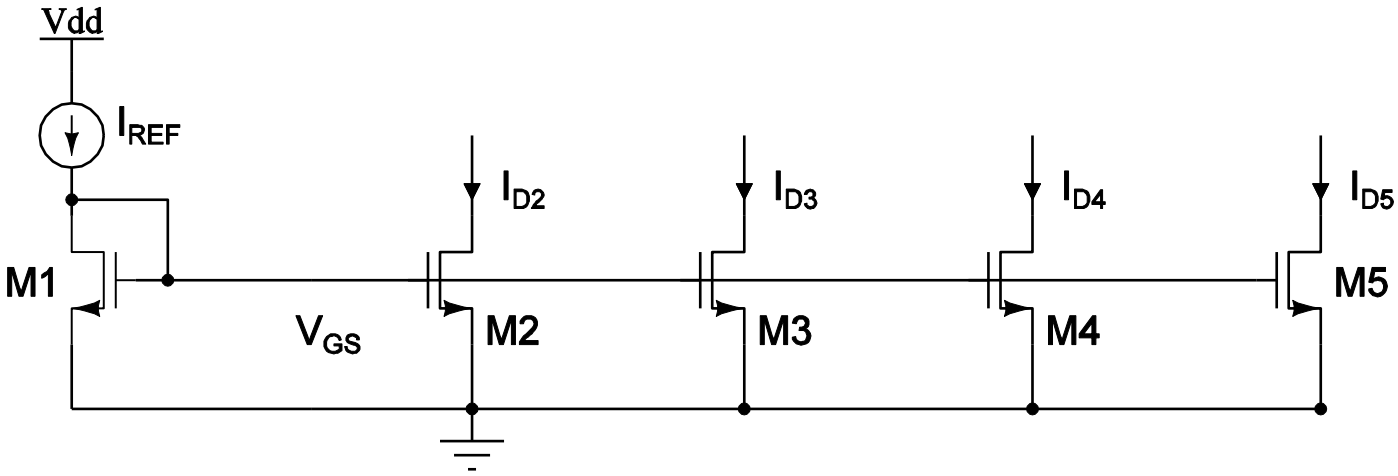
- Allows precise copying of the current with no dependence on process and temperature

General Concept of Current Mirror

- Basic current mirror concept: I → V → I
- Define current gain: $\alpha = \frac{I_{OUT}}{I_{IN}}$
- Small-signal output resistance R_O.
- Minimum output voltage V_{Omin}.



Current Mirrors



- More generally, we can connect more transistors to make several output currents.
- Every transistor shares the same V_{GS}, hence same V_{OD}.
- By designing different size of the transistor, we can mirror out different currents from the reference current. Here channel length modulation effect is neglected.

$$I_{Dn} = \frac{\left(W/L\right)_n}{\left(W/L\right)_1} I_{REF}$$

Current Mirror Specifications

- Small-signal output resistance R_O.
- Minimum output voltage V_{Omin}.
- Current gain error definition:

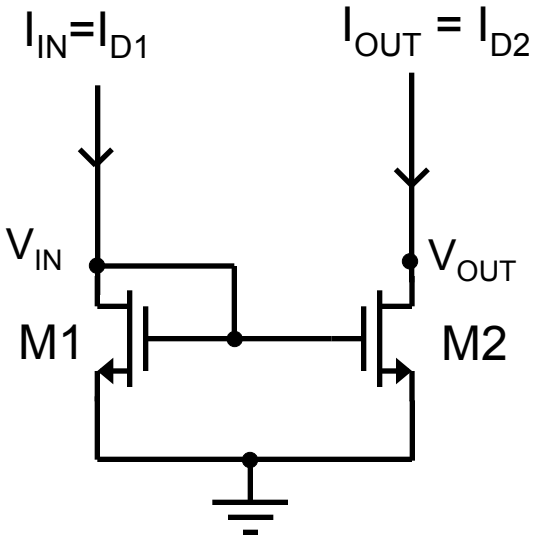
$$E = \frac{I_{OUT} - I_{OUT\_ideal}}{I_{OUT\_ideal}}$$

- Two types of error:
  - systematic error: error caused by circuit structure.
  - Random error: error caused by process variations.
- These two types of error are commonly seen in many analog circuits.
- A robust design is to minimize both systematic error and random error.

Current Mirror Analysis

- As $V_{GS1} = V_{GS2}$ and assuming matched $V_{TH1} = V_{TH2}$

$$\frac{I_{OUT}}{I_{IN}} = \frac{\left(W/L\right)_2 (1+\lambda V_{OUT})}{\left(W/L\right)_1 (1+\lambda V_{IN})}$$



- The output resistance of current source is the output resistance of M2

$$R_O = \frac{1}{\lambda I_{D2}} = \frac{1}{\lambda I_{OUT}}$$

- Normally, larger L is used so that λ effect is reduced and the output resistance is higher.
- The current gain systematic error is:

$$I_{OUT\_ideal} = \frac{(W/L)_2}{(W/L)_1} I_{IN}$$

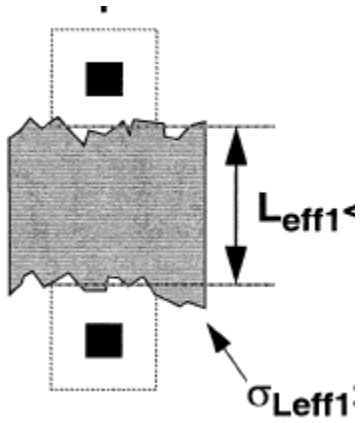
$$E = \frac{I_{OUT} - I_{OUT\_ideal}}{I_{OUT\_ideal}} = \frac{(1+\lambda V_{OUT})}{(1+\lambda V_{IN})} - 1 = \frac{\lambda}{(1+\lambda V_{IN})}(V_{OUT} - V_{IN}) \approx \lambda (V_{OUT} - V_{IN})$$

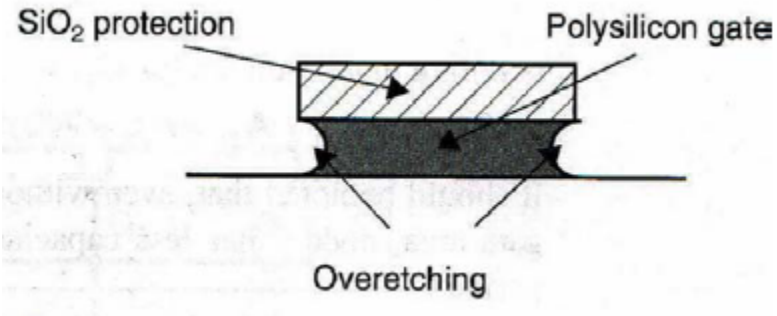
Current Mirror Analysis-Gate Overdrive

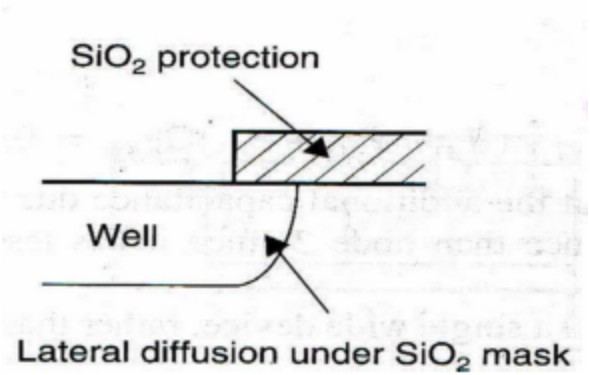
- This current relationship will be true as long as M2 is in saturation. Clearly, this will happen when $V_O=V_{DS2} > V_{OD2}$
- Gates of two transistors are connected: $V_{GS2} = V_{GS1}$ so $V_{GS2} – V_{TH2} = V_{GS1} – V_{TH1}$ as $V_{TH1} = V_{TH2} \rightarrow V_{OD1}=V_{OD2}$
- Define the minimum output voltage: $V_{Omin} > V_{GS2} – V_{TH2} = V_{OD}$
- Hence it is a benefit to have a low gate overdrive to increase the output swing.
- How much should the gate overdrive be?
- For same drain current, if the overdrive is small, transistor size will be very large, giving area penalty and speed penalty.
- Overdrive voltage is a trade-off between speed and minimum output swing. Typically, overdrive is selected between 0.1-0.4V.

Mismatch

- Matched device means all the devices are designed having matched parameters.
- Mismatch: parameter differences between matched devices
  - Random statistical fluctuations
  - Process bias
  - Patten shift (Mask misalignment)
  - Diffusion interactions



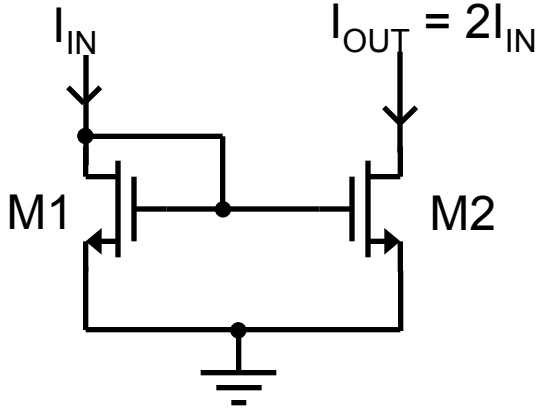




Current Mirror Mismatch

- A current mirror with current ratio of two is designed. Assume $V_{IN}=V_{OUT}$ to eliminate the channel length modulation effect.
- Due to mismatch between M1 and M2, the output current is not exactly two times of the input current.
- 3 ways to implement:
  - A: $W_2=W_1$, $L_2=0.5L_1$
    - λ mismatch

$$\frac{I_{OUT}}{I_{IN}}=\frac{\left(W/L\right)_2(1+\lambda_2 V_{OUT})}{\left(W/L\right)_1(1+\lambda_1 V_{IN})}\neq 2$$

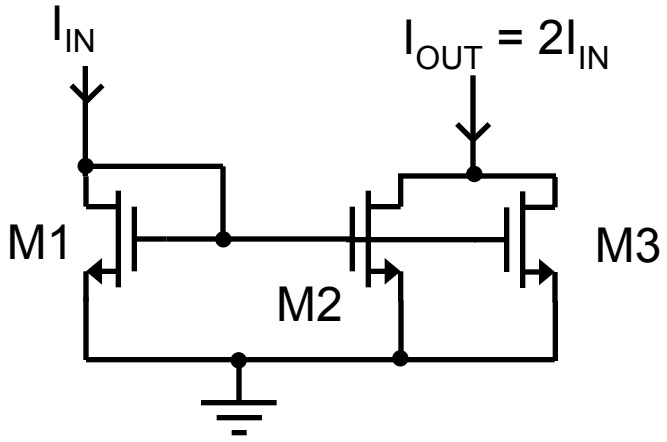


  - B: $W_2=2W_1$, $L_2=L_1$
    - ΔW and ΔL mismatch

$$\frac{I_{OUT}}{I_{IN}}=\frac{\dfrac{2W+\Delta W}{L+\Delta L}}{\dfrac{W+\Delta W}{L+\Delta L}}\neq 2$$

  - C: Two transistors in parallel, $W_3=W_2=W_1$, $L_3=L_2=L_1$
    Best solution

$$\frac{I_{OUT}}{I_{IN}}=\frac{\dfrac{2(W+\Delta W)}{L+\Delta L}}{\dfrac{W+\Delta W}{L+\Delta L}}=2$$



Eliminate the Systematic Error

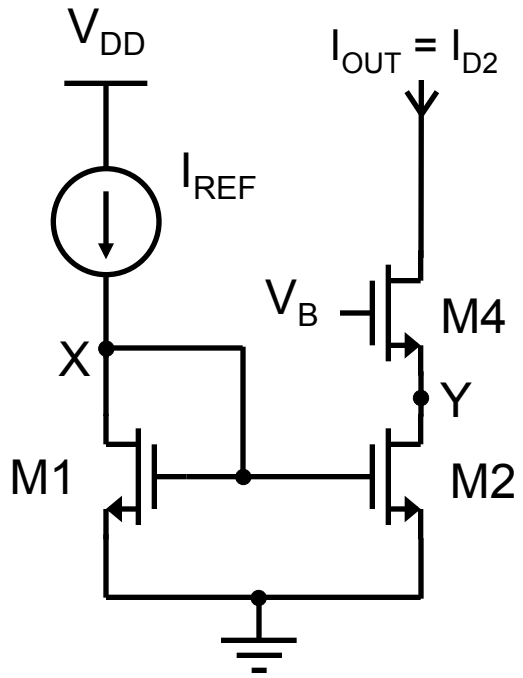
- As we have seen, first simple current mirror output current ($I_{OUT} = I_{D2}$) changes when the drain voltage of M2 changes. From model parameter $\lambda = 0.05$, the change in I_{OUT} for a 1V change in V_{D2} will be 5%, which is not acceptable in many analog applications.
- Can we do something about this?

$$E = \frac{I_{OUT} - I_{OUT\_ideal}}{I_{OUT\_ideal}} = \frac{(1+\lambda V_{OUT})}{(1+\lambda V_{IN})} - 1 \approx \lambda(V_{OUT} - V_{IN})$$

- The key to eliminate the current gain systematic error is to make V_{OUT}=V_{IN} in the simple current mirror.
- A straightforward way to achieve this would be having an extra MOSFET in series with M2 and fix the drain voltage of M2 to V_{IN}. This extra transistor is called cascode transistor.

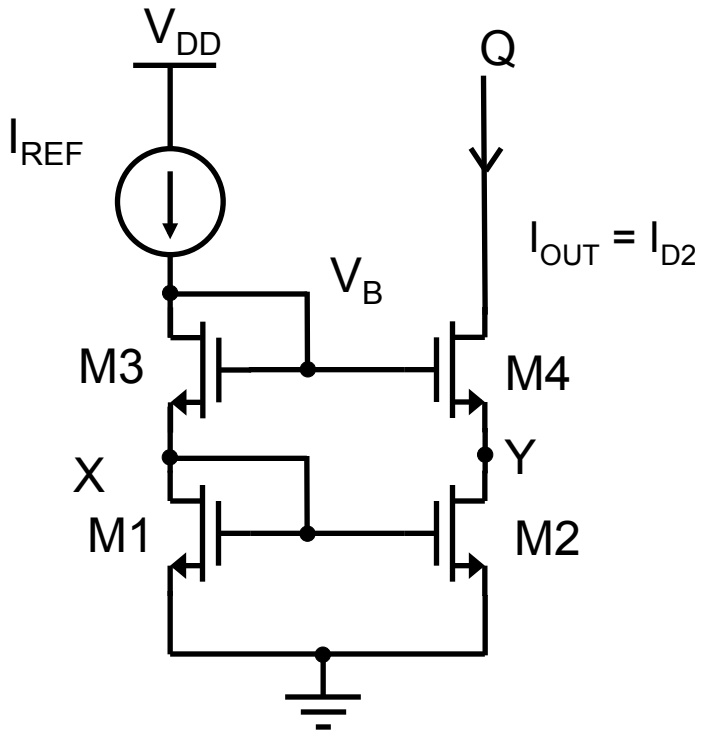
Cascode Current Mirror

- If we choose $V_B = V_{GS4} + V_X$,
  then $V_Y = V_B - V_{GS4} \rightarrow V_Y = V_X$.
- If V_X and V_Y are the same, the channel length modulation term for both M1 and M2 will be the same. Hence, the effect is corrected.
- M4 now shields I_{out} from voltage variations at the output node as V_Y is fixed by transistor M4 and does not depend on V_{OUT}, eliminating the systematic error: channel length modulation mismatch.
- The cascode transistor M4 normally has the same size as M2.
- This current mirror is called cascode current mirror.



Cascode Current Mirror

- How to generate the required V_B?
- One simple way would be to create an exact replica of M4 in the left branch using a diode connected transistor M3 and utilize the gate voltage of M3 as V_B.

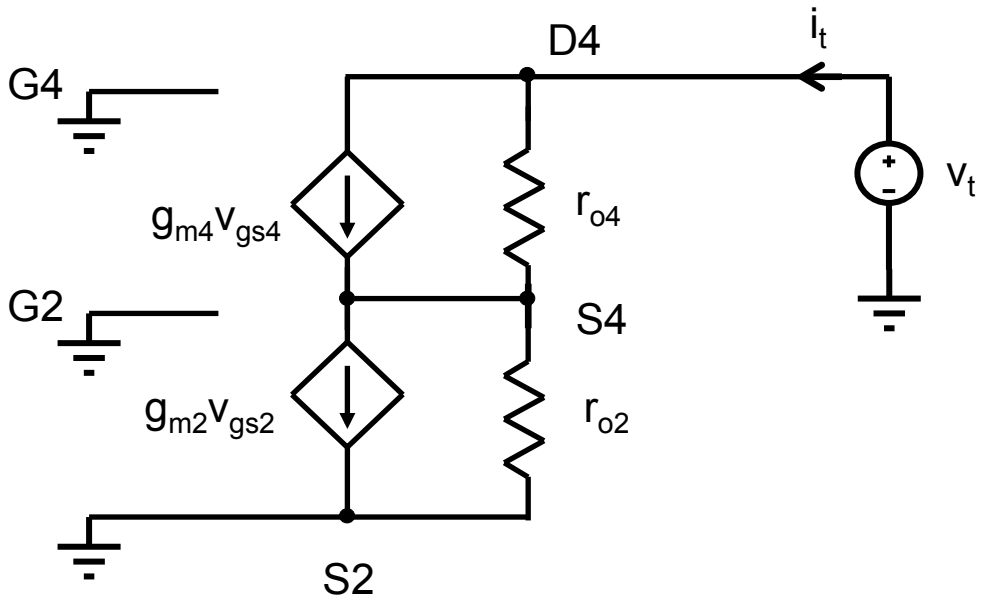


Cascode Current Mirror

- Transistor M1 and M3 will have the same overdrive V_{OD}.
- M2 and M4 have the same overdrive.
- As mentioned before, M1 and M2 have the same overdrive. So all 4 transistors have the same overdrive V_{OD}.
- Note all 4 transistors have the same threshold voltage V_{TH} if body effect is ignored.
- Hence $V_X = V_Y = V_{TH} + V_{OD}$
- $V_{GS3} = V_{OD} + V_{TH}$ as M1 and M3 carry the same current.
- $V_{G3} = V_{GS3} + V_X = 2\,V_{TH} + 2\,V_{OD}$ ignoring body effect.
- Hence $V_{G4} = 2\,V_{TH} + 2\,V_{OD}$
- This should also be the case with body effect – only 2 V_{TH} will become $V_{TH1} + V_{TH3}$.

Cascode Current Mirror-Output Resistance

- The output resistance of this current mirror can be found using low frequency small signal equivalent circuit. A small signal is applied at the drain of M4 to find R_O. The method as the same in EE2005 where a test voltage v_t is applied at the point where effective resistance is to be found and then current through the test source, it is calculated so that $R_O=v_t/i_t$.
- We will neglect g_{mb}. Only modified result will be given later.



Cascode Current Mirror-Output Resistance

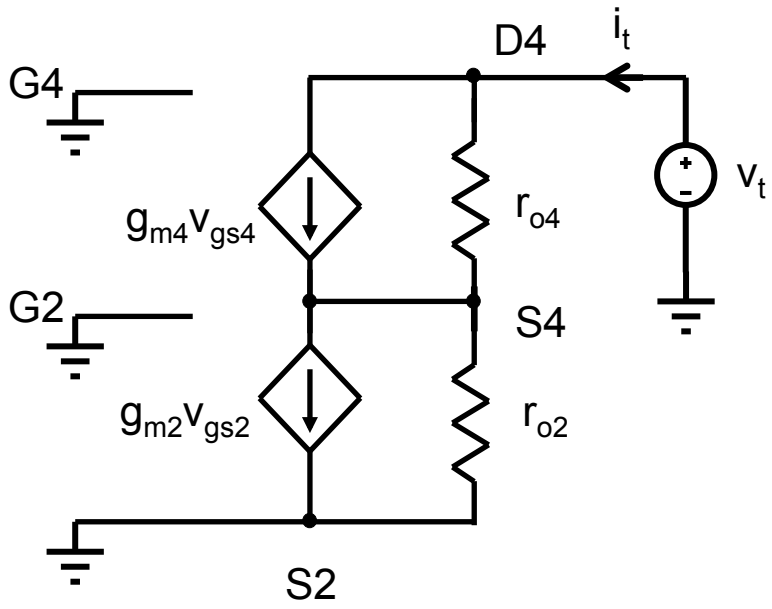
- Since the gate voltages of M2 and M4 are fixed by M1and M3 and there is no variable voltage at M1 and M3, the gates of M2 and M4 are AC ground.
- Clearly, $v_{gs2}=0$, $v_{gs4} = - i_t r_{o2}$

$$i_t = \frac{v_t - v_{s4}}{r_{o4}} - g_{m4} i_t r_{o2}$$

$$i_t(1 + g_{m4} r_{o2}) = \frac{v_t - i_t r_{o2}}{r_{o4}}$$

- Hence, R_O = output resistance of single cascode current mirror

$$R_O = \frac{v_t}{i_t} = r_{o4}(1 + g_{m4} r_{o2}) + r_{o2}$$



Cascode Current Mirror-Output Resistance

- This type of result is quite generally applicable in the sense that due to presence of M2 below M4, the output resistance seen at the drain of M4 is magnified by a factor (1 + g_{m4} r_{o2}). We will use this result later whenever such a configuration appears.
- Typically, g_{m4} r_{02} >> 1 and r_{02} = r_{04} = r_0 as M2 and M4 carry the same current.

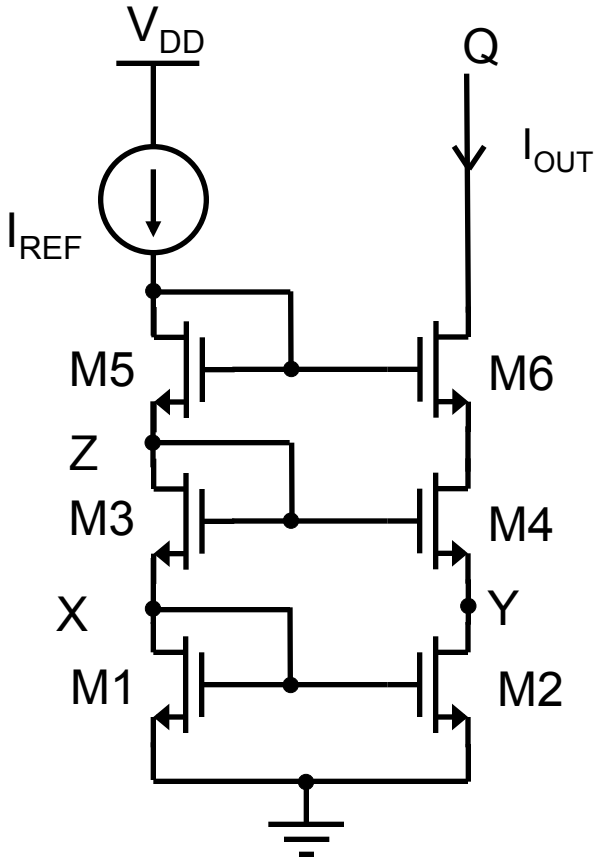
$$R_O = g_{m4} r_{o2}^2$$

- If body effect is included: $R_O = (g_{m4} + g_{mb}) r_{o2}^2$
- Features of Cascode current mirror:
  - No current gain systematic error.
  - Higher output resistance.
  - Higher minimum output voltage.

Triple Cascode Current Mirror

- A variation of this circuit known as triple Cascode current mirror where a device is added on the left and right is also possible. R_O in this case will be

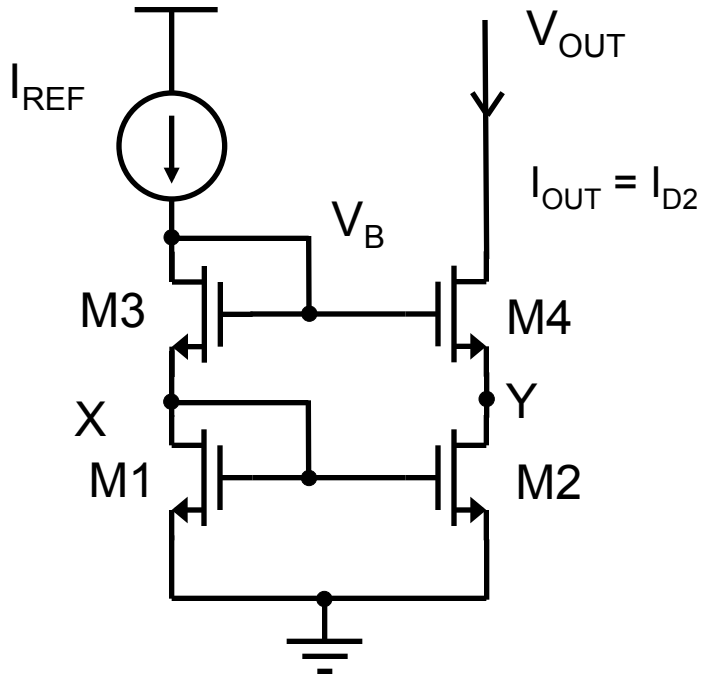
$$
\begin{aligned}
R_O &= r_{o6}\left\{1 + g_{m6}\left[r_{o4}\left(1 + g_{m4}r_{o2}\right) + r_{o2}\right]\right\} \\
&\quad + r_{o4}\left(1 + g_{m4}r_{o2}\right) + r_{o2} \\
&= g_{m6}g_{m4}r_o^3 \\
&\approx r_o\left(g_m r_o\right)^2
\end{aligned}
$$



Minimum Output Voltage

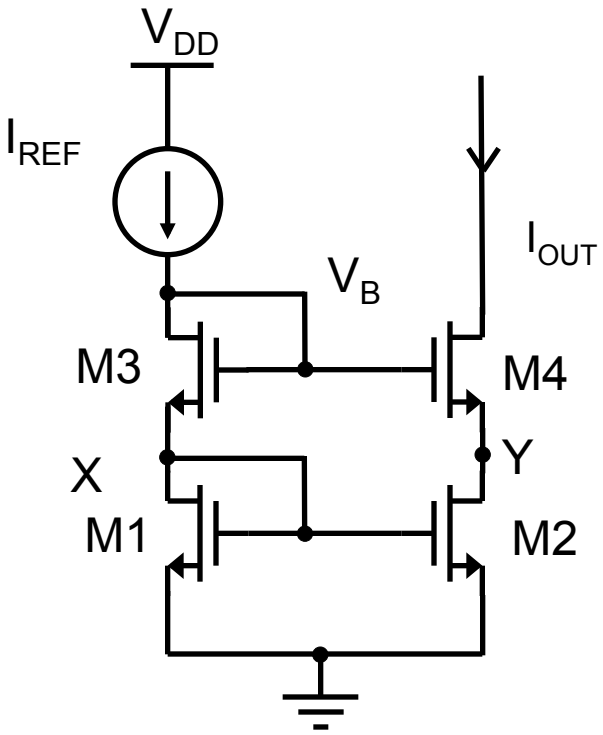
- Returning to the 4 MOSFET circuit, if body effect is present, V_{TH2} and V_{TH4} will be different and voltages will alter, but concept still works. For the concept to work, M2 and M4 both must be in saturation, i.e.

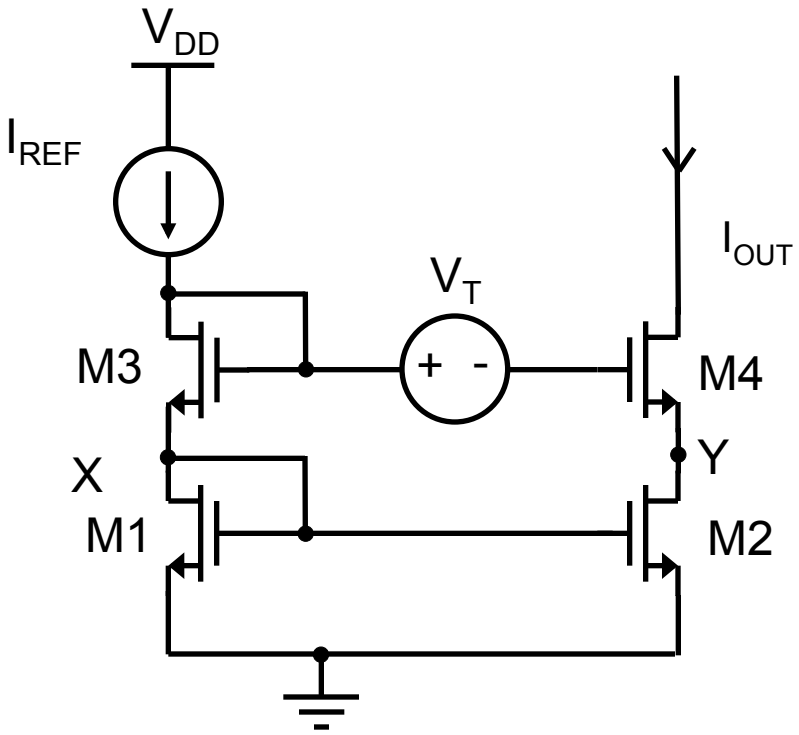
  $V_X = V_Y = V_{TH} + V_{OD}$ and M4 must be in saturation region: $V_{DS4} > V_{OD}$
- So $V_{OUT} > V_T + 2\,V_{OD}$
- Hence V_{OUT} needs to be quite high, over 1V, for proper operation. This could be a problem for low voltage design and will certainly reduce output swing.
- A level shift follower is introduced and this voltage requirement can be reduced to $2\,V_{OD}$.



Low Voltage Cascode Current Source 1

- In cascode current mirror, $V_X=V_Y$ and $V_X=V_{TH}+V_{OD}$ → $V_{Omin}=V_{TH}+2V_{OD}$
- If $V_X \neq V_Y$ → Low output voltage, high swing
- Adding a voltage shifter V_{TH}, now $V_Y=V_X-V_{TH}=V_{OD}$





Low Voltage Cascode Current Source 1

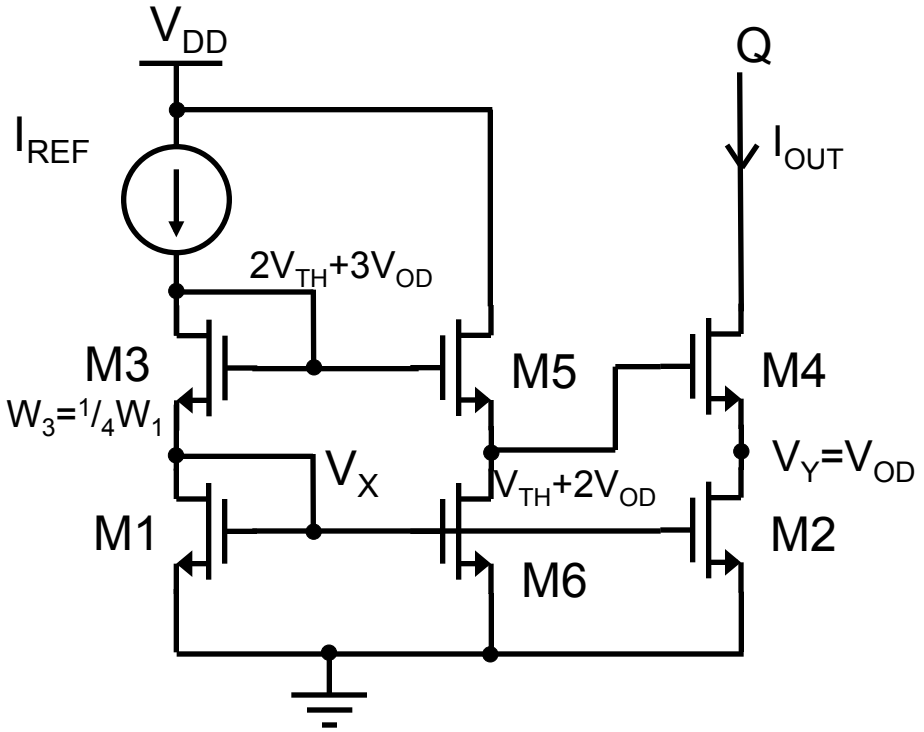
- All transistors have the same overdrive except M3. $V_X=V_{TH}+V_{OD}$
- Since W3=1/4W1, $I_{REF}=\frac{1}{2}\mu C_{OX}\frac{1}{4}\left(\frac{W}{L}\right)(V_{GS3}-V_{TH})^2=\frac{1}{2}\mu C_{OX}\left(\frac{W}{L}\right)V_{OD}^2$

$V_{GS3}=V_{TH}+2V_{OD}$ → $V_{G3}=V_X+V_{GS3}=2V_{TH}+3V_{OD}$

$V_{G4}=V_{TH}+2V_{OD}$ →

$V_Y=V_{OD}$

$V_{Omin}=2V_{OD}$



Low Voltage Cascode Current Source 1

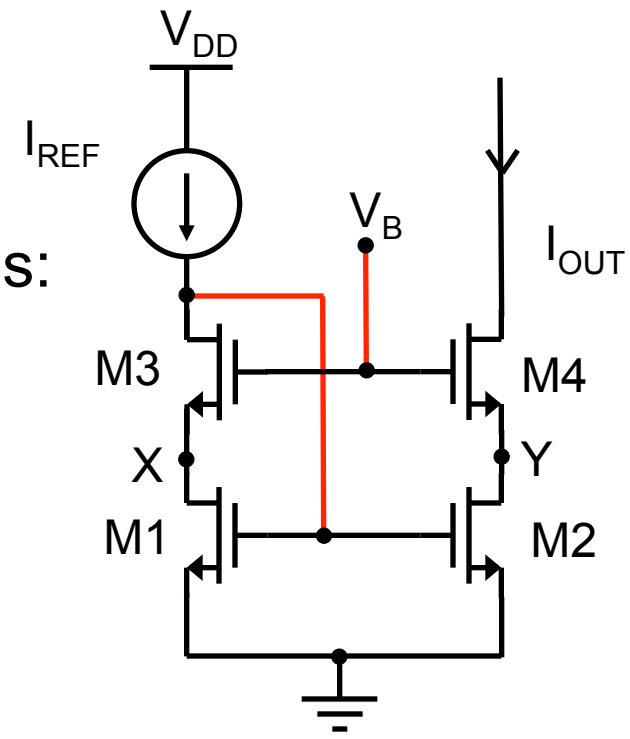
- The minimum output voltage is now $2V_{OD}$.
- The output resistance remains the same as the Cascode current mirror.
- However, since $V_X=V_Y$ is no longer valid, the current gain systematic error is not zero.

$$E \approx \lambda(V_Y - V_X) = -\lambda V_{TH}$$

- This drawback can be eliminated by another circuits, i.e. low voltage Cascode current mirror circuit 2.

Low Voltage Cascode Current Source 2

- All the transistors have the same overdrive. Set $V_B=V_{TH}+2V_{OD}$
- $V_X=V_Y=V_B-(V_{TH}+V_{OD})=V_{OD}$
- Then the minimum output voltage is: $V_{OUT}=2V_{OD}$
- And since $V_X=V_Y$ → no current gain systematic error.
- Design all transistors' overdrive smaller than its V_{TH}.
- Since $V_{DS3}=V_{GS1}-V_{DS1}=V_{TH}>V_{OD}$ → M3 at saturation region.
- All transistors are at saturation region.

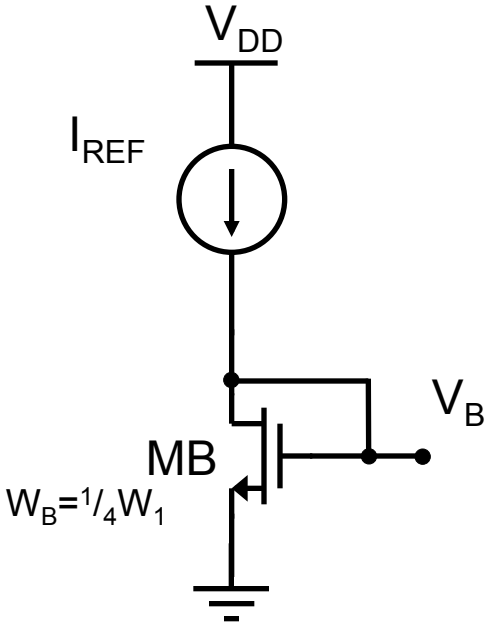


Low Voltage Cascode Current Source 2

- The low voltage cascade current source 2 has:
  - High output resistance
  - Low output voltage: $V_{OUT}=2V_{OD}$
  - No current gain systematic error.
- How to generate $V_B=V_{TH}+2V_{OD}$?
- Two ways:
  - Assuming same L for all transistors,
  - Since $W_B=1/4W_1$ and same current

$$I_{REF}=\frac{1}{2}\mu C_{OX}\frac{1}{4}\left(\frac{W}{L}\right)(V_B-V_{TH})^2=\frac{1}{2}\mu C_{OX}\left(\frac{W}{L}\right)V_{OD}^2$$

  - $V_B=V_{GS1}=V_{TH}+2V_{OD}$



Low Voltage Cascode Current Source 2

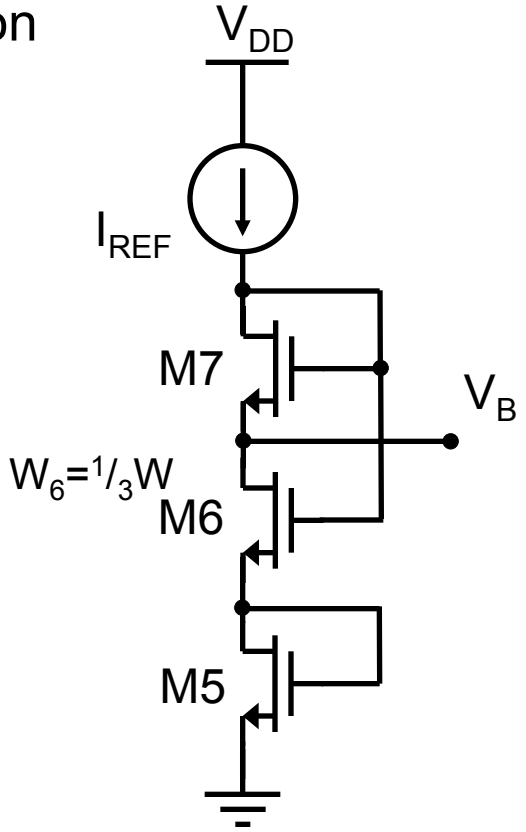
- Another way to generate V_B:
- All transistor have the same overdrive except M6.
- $V_{DS6}=V_{GS6}-V_{GS7} \rightarrow V_{GS6}=V_{DS6}+V_{GS7}$
- Since $V_{GS7}>V_{TH}$, $V_{DS6}<V_{GS6}-V_{TH} \rightarrow$ linear region
- $V_{GS6}-V_{TH}=V_{DS6}+V_{GS7}-V_{TH}=V_{DS6}+V_{OD}$

$$I_{D6}=\frac{1}{3}\frac{W}{L}\mu C_{OX}\left[(V_{GS6}-V_{TH})\cdot V_{DS6}-\frac{1}{2}V_{DS6}^2\right]$$

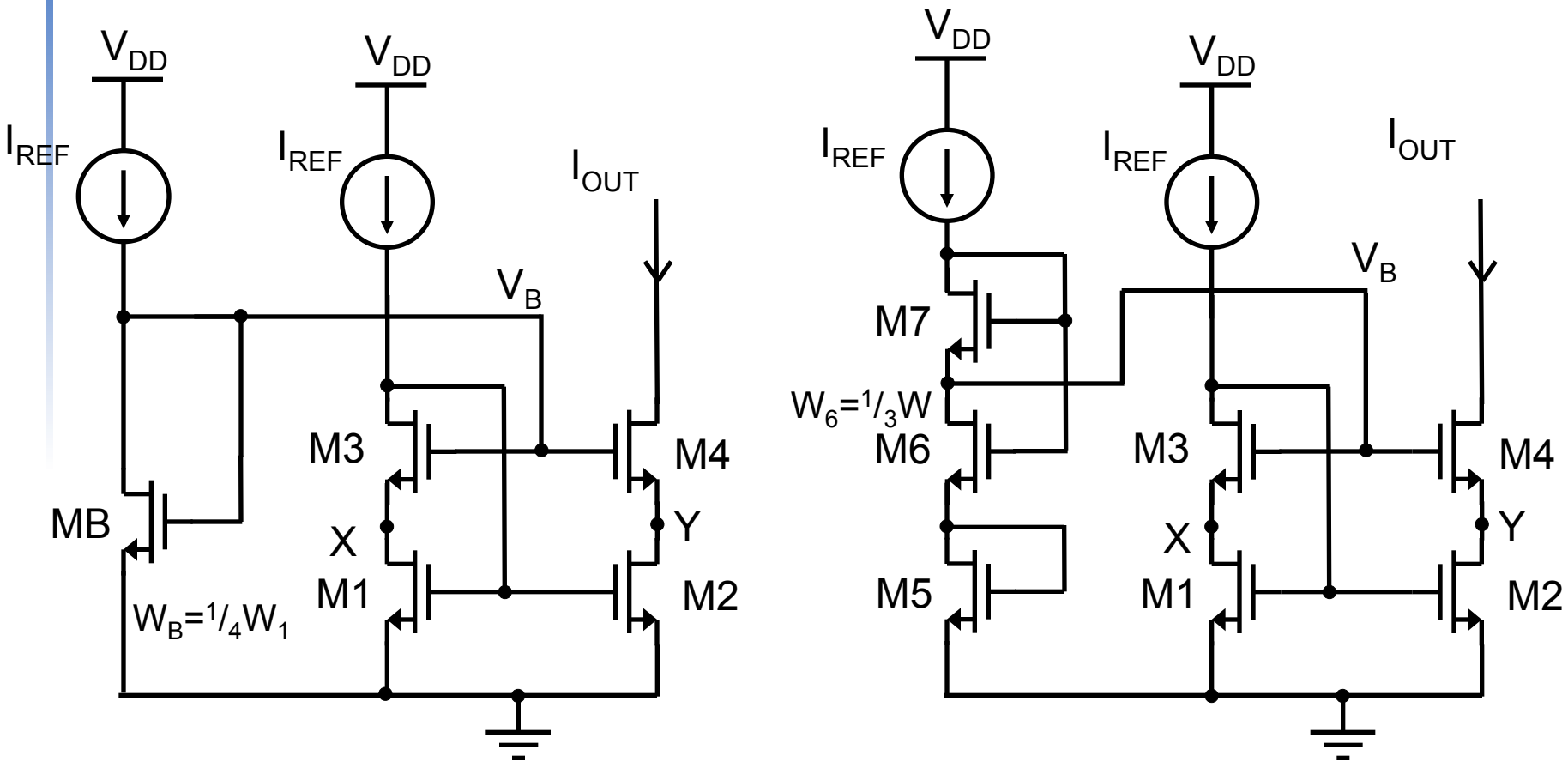
$$I_{D7}=\frac{1}{2}\frac{W}{L}\mu C_{OX}V_{OD}^2$$

$$I_{D6}=I_{D7} \qquad and \qquad V_{GS6}-V_{TH}=V_{DS6}+V_{OD}$$

- Solve the equations: $V_{DS6}=V_{OD}$
- $V_B=V_{GS5}+V_{DS6}=V_{TH}+2V_{OD}$



Low Voltage Cascode Current Source 2



Full schematic of two types of low voltage Cascode current mirror 2.

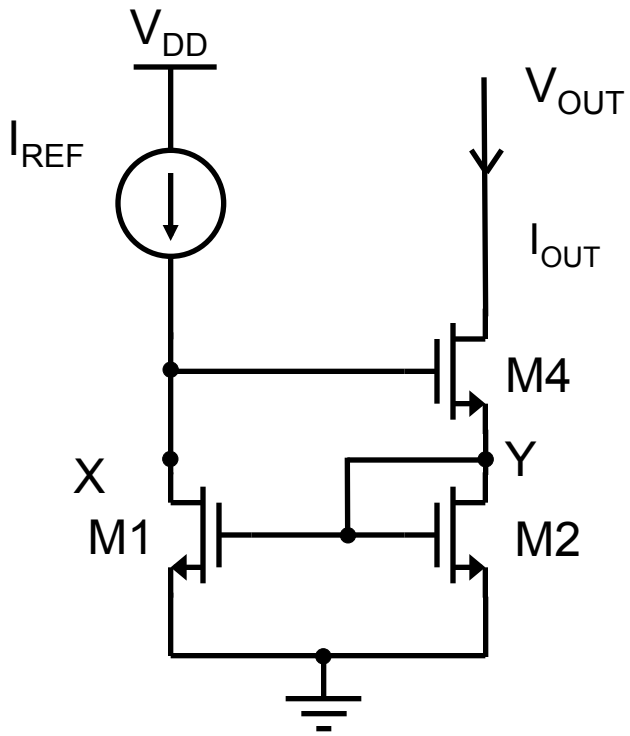
Wilson Current Mirror

- Transistor M1 and M2 have the same overdrive:

$$\frac{I_{OUT}}{I_{IN}} = \frac{\left(W/L\right)_2(1+\lambda V_Y)}{\left(W/L\right)_1(1+\lambda V_X)}$$

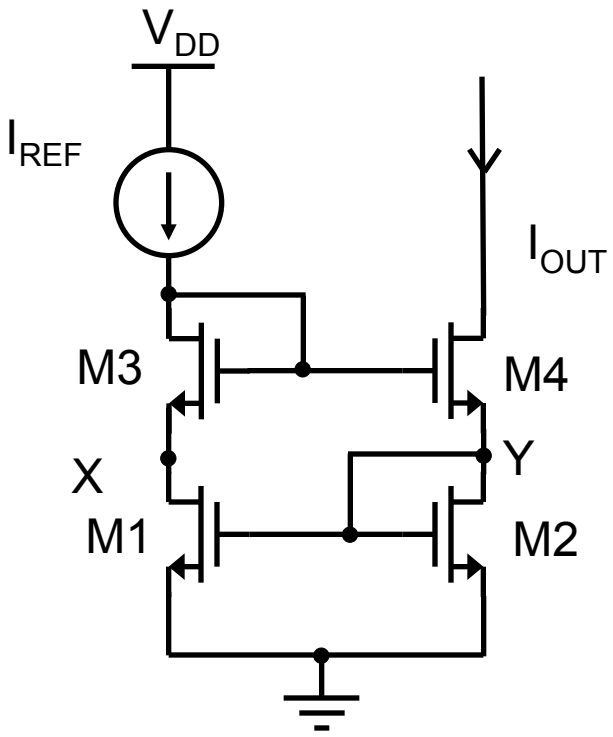
- Use feedback to stabilize the output current.
- $V_{OUT}\uparrow \rightarrow I_{OUT}\uparrow \rightarrow V_Y\uparrow \rightarrow V_X\downarrow \rightarrow I_{OUT}\downarrow$
- High output resistance: $g_m r_o^2$
- Minimum output voltage: $V_{TH}+2V_{OD}$
- Since $V_X \neq V_Y$, the current gain systematic error is not zero.

$$E \approx \lambda(V_Y - V_X)$$



Wilson Current Mirror

- By adding M3, $V_X=V_Y$, the current gain systematic error is zero.
- High output resistance: $g_m r_o^2$
- Minimum output voltage: $V_{TH}+2V_{OD}$
- Not good for low-voltage design



Current Mirror Summary