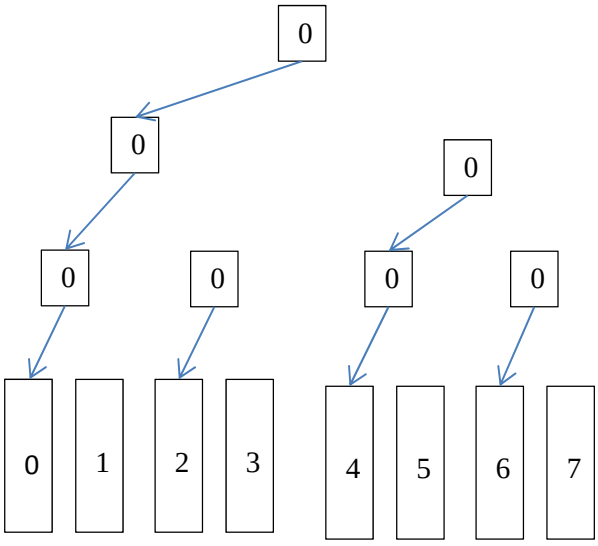
York University

Lassonde School of Engineering

EECS4201

Assignment 1

1. Problem 1.12
2. Problem 1.15
3. Problem 1.17
4. Write a C/Java/Any_language program to implement both LRU and Pseudo LRU algorithm for block replacement in the cache. The input to the simulator is N (associativity 4, 8, or 16) and a sequence of numbers 0 to N-1. The output is a sequence of numbers indicating the number of the block in the LRU position. Assume that you start with a state like the one shown below (o means left) for 8-way set associative



5. Consider a processor that consumes 80 W (25% of them leakage power), and 1.3V. The processor uses DVFS and V can go down to 1V (that of course include DVS). The voltage can go down to 1V, but not anymore. You have to build a computer using that CPU. The restriction is max power consumption of 55W. Is it possible to do this? If No explain why, if yes what is the voltage and frequency? how fast (or slow) the new system to the original one?