York University

Dept. of Computer Science and Engineering

EECS4201
Computer Architecture
Quiz 1
Oct. 13 2016
Time allowed: 25 minutes

Question 1 – 6 points

Consider a DRAM where it takes 20ns to read a row into a row buffer, 20ns to send the row from the row buffer to the ship's pins, and 20ns for pre-charge. Write the time at which the following memory requests are completed. By completed we mean sent to the chip pins. Consider both open page and close page policy. Note that X, X+1, X+2 maps to the same row, Y, Y+1, Y+… maps to a different row in the same bank

Request	Time of arrival	Completion time	
		Open page	Closed page
X	0ns		
Y	10 ns		
X+1	100		
X+2	200		
Y+1	250		
X+3	300		

Question 2 – 4 points

Assume a write-back split cache with miss rate of 2% for instruction cache and 5% for data cache. The main memory access time is 200 cycles. Assume that 20% of the instructions are load and 15% are store.

a) What is the average number of stall cycles per instruction due to cache miss for both instructions and data assuming the probability of a dirty block is 10%?
b) What is the average number of stall cycles per instruction if the cache is write-through with no write buffer?