Dept. of Computer Science and Engineering
EECS3215 – Embedded Systems

ADC

Lab 6

Objectives:

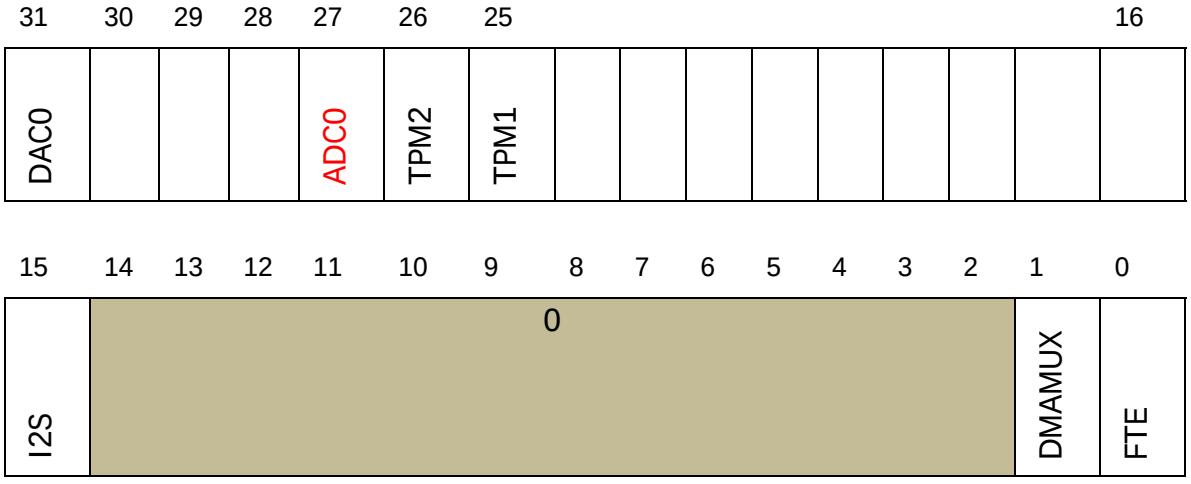
To learn how to use the ADC unit and to interface the board to a sensor and 7-segment display;

ADC

First, red the class notes about the ADC.

The KL43Z has one ADC (ADC0) with 16 chanells. In order to configure and use the ADC, you have to setup some registers., her are these registers

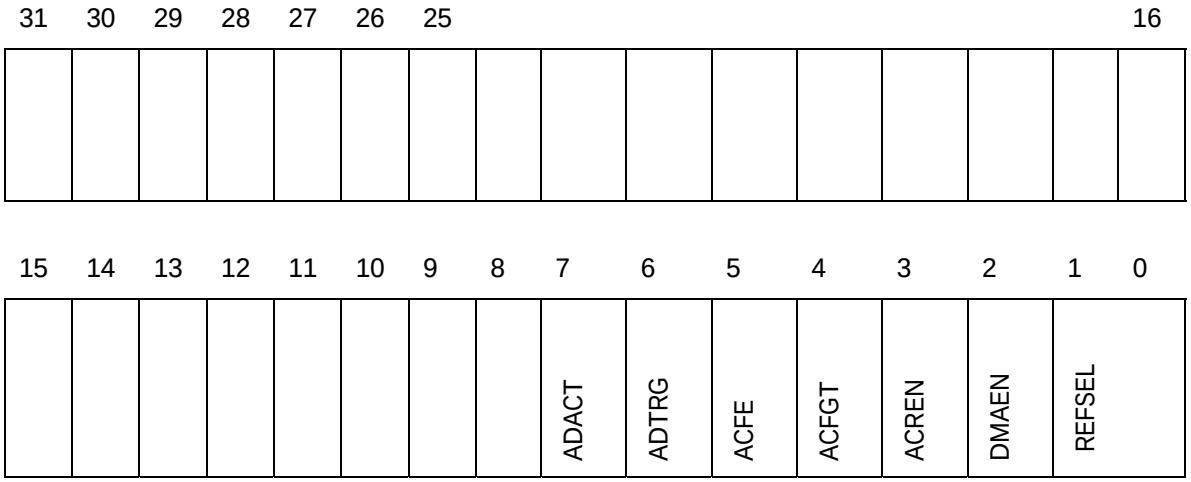
SIM_SCGC6 Enabling the ADC



In order to enable the clock to the ADC0 module, set bit 27 (ADC0) to 1.

Start Conversion trigger ADC0_SC2

The Status and Control Register 2 has the following format

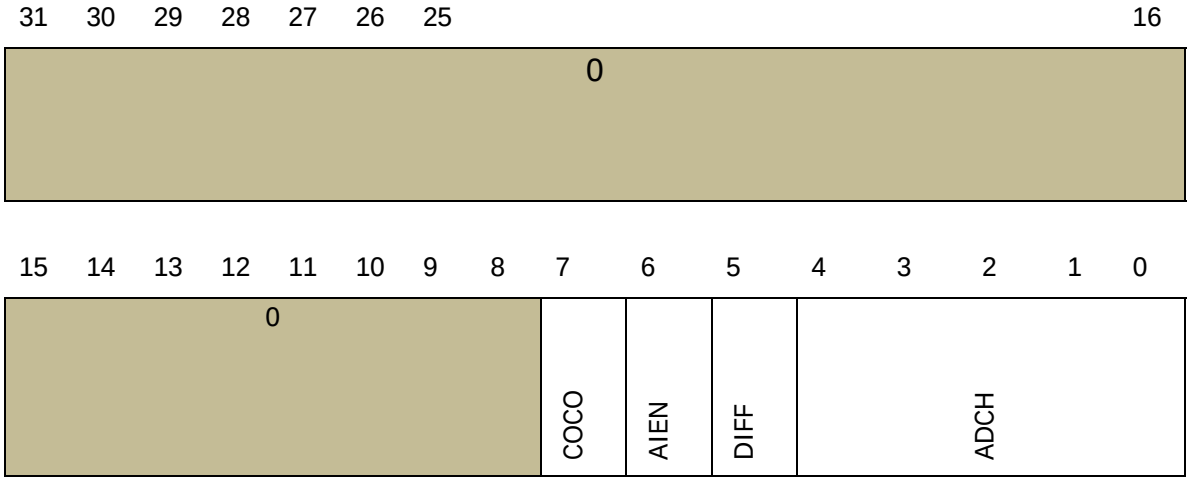


The important fields are

ADACT (bit 7)	Conversion in progress (1) not in progress (0)
ACFE	
ADTRG (bit 1)	software trigger (0) hardware trigger (1)
REFSEL	Voltage reference select
	00 default V_{ref} V_{REFH} and V_{REFL}

Input channel ADC0_SC1A

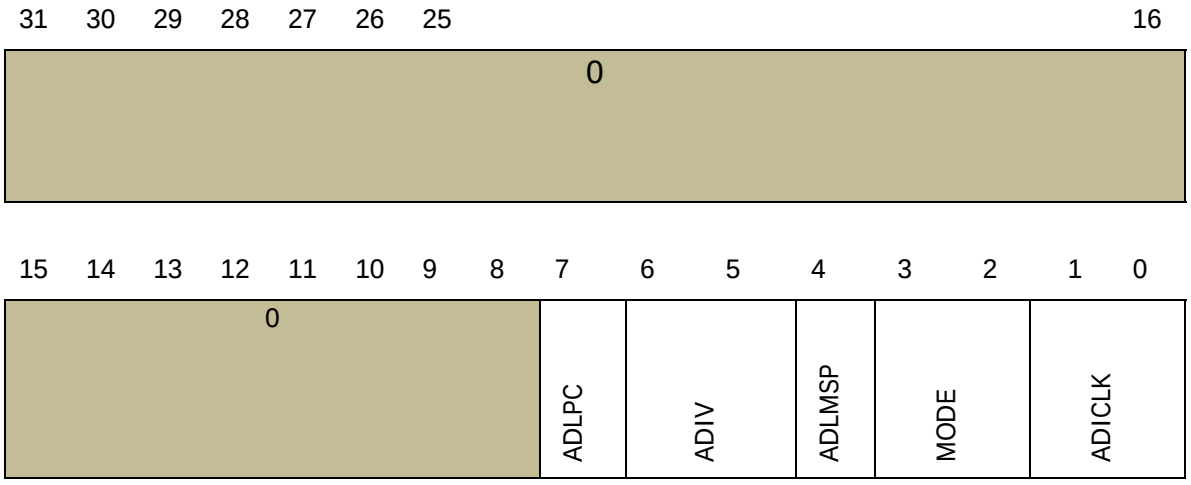
Note that only SDC0_SC1A can be used in software triggering (no 1B). Also ADC0_SC1A is referred to as **ADC0->SC1[0]**



The important bits are

COCO(7)	Conversion complete flag.
	It is a read only bit, set each time the conversion is completed only when the compare function (bit 5 of SC2 –ACFE--) is 0 and the hardware average function is disabled AVGE in SC3. It is cleared when the data is read
AIEN	0 Conversion complete interrupt is disabled
	1 Conversion complete interrupt is enabled
DIFF	0 Single ended conversion
	1 Differential conversion
ADCH	See the manual, what we need is
	0000 When DIFF=0, DADP0 is the input, else DAD0 is the input

ADC Configuration Register 1 ADC0_CFG1



The important fields are

ADLPC(7) Low power configuration

ADIV(6-5) Clock divide select

00 Ratio is 1, rate = clock rate

01 Ratio is 2, rate = clock/2

10 Ratio is 4

11 Ratio is 8

ADLSMP Sample time configuration to allo long sample time for high impedance input

MODE(3-2) DAC resolution mode

00 When DIFFF=0, single ended 8-bit conversion

01 When DIFF=0, 12- bit conversion

10 When DIFF=0, 10-bit conversion

11 When DIFF=0, 16-bit conversion

ADICLK(1-0) CLOCK speed

00 Bus clock

01

10

11

ADC0_RAor ADC0->R[0] is where the data is stored

LAB

In this lab you will interface an IR sensor to the FRDM-KL43z board and you will show the sensor output on a 2 7-segment displays.

Deliverables

Demo the program to the TA, A lab report is due march 12.

The sensor is shown here www.robotshop.com/ca/en/sharp-gp2y0a21yk0f-ir-range-sensor.html

You might get an older version https://www.pololu.com/product/1136

The 7-segment display https://store.digilentinc.com/pmod-ssd-seven-segment-display