York University
Lassonde School of Engineering
Dept. of Electrical Engineering and Computer Science
Winter 2019

EECS3215	**Midterm**	**Embedded Systems**
Thursday, Feb. 28th 2019		4:00 – 5:00

Last Name _____ First name _____

ID _____

Instructions to students:

Answer all questions.
Marks are shown in front of each question number.
Show your work
Be neat and clean while drawing your logic, block, or state diagrams.

This examination consists of **5** questions

Problem	Points
1	/7
2	/5
3	/6
4	/5
Total	/**23**

Problem 1 (3+2+2 points)

a) Compare between interrupt and polling methods in serving input ports, what are the advantages and disadvantages for each

Interrupt:

- **Doesn't waste time polling**
- **Needs context switching for ISR**

Polling:

- **Periodically polls, may be no need**
- **No context switching (faster for small tasks)**

b) Write a pseudo code for a program that serves 2 input ports using polling

```
while(1) {
     Check port 1
     if(ready) {process the data}
     Check port 2
     if (ready) {process data}
}
```

c) Can we have a priority in polling, how or why not?

Yes, we can we can poll one port (high priority one) more than once in a polling cycle

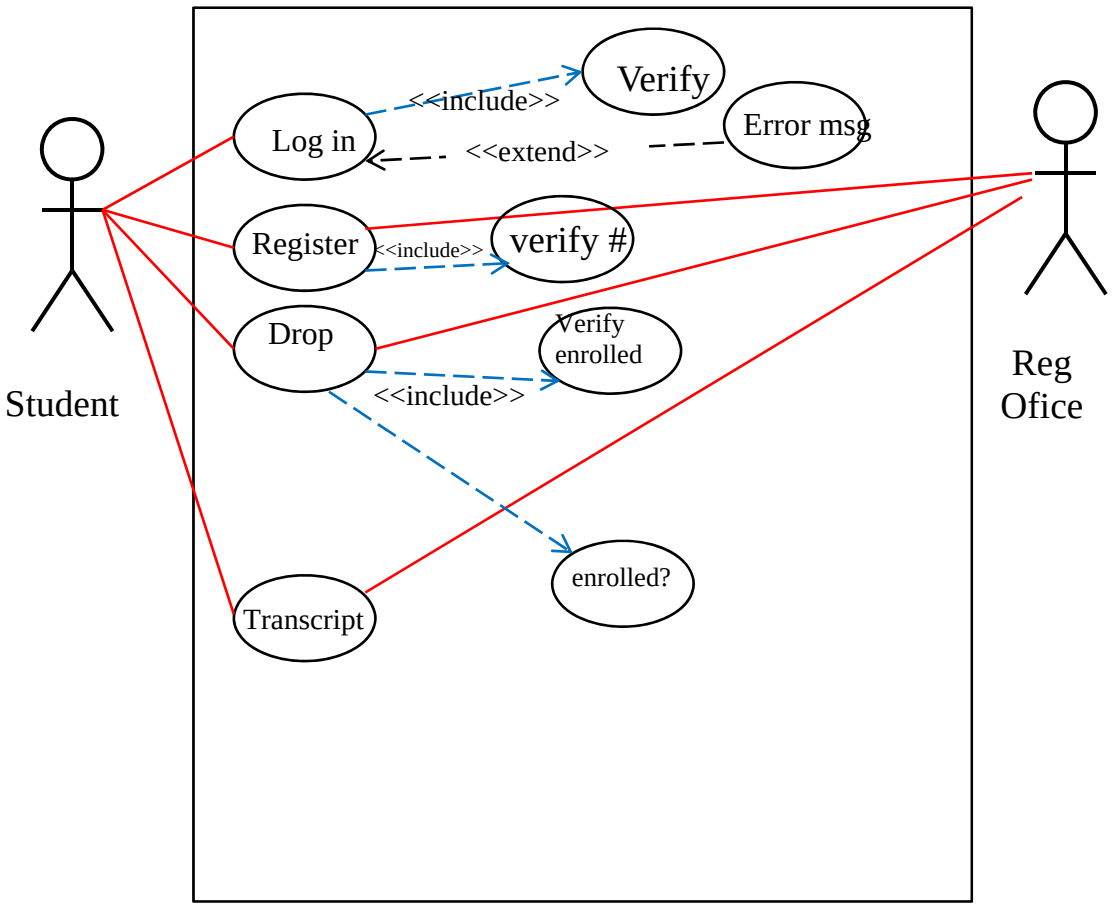
```
while(1) {
     Check port 1
     if(ready) {process the data}
     Check port 2
     if (ready) {process data}
     check port 1
     if ready {Process data}
     check port 2
     if ready {Process data}

     check port 1
     if ready {Process data}
     check port 3
     if ready {Process data}
}
```

Problem 2 (5 points)

Draw a simple use case diagram to model the student course registration in a university.
The student interaction with the system is limited to
Registering in a course
Dropping a course
Getting a transcript with the courses registered in

The system checks seat availability and pre-requisites checking

This is just one way of representing it, some changes are possible



Problem 3 (3+3 points)

a) What is the difference between direct mapped cache and N-way set associative cache? Briefly explain

In direct mapped, there is only one location a block can go to in the cache
N-way set associative, there are N different locations for the block to go to

b) Consider a direct mapped cache with 128KB of data and 128 Bytes block size

What block numbers these byte addresses are mapped to?
128KB/128 = 1 KB which is 10 bits for the block
7 bits for the byte in the block

1024 (0x00400) **000OOOOOO1OOO0000000 → block 8**

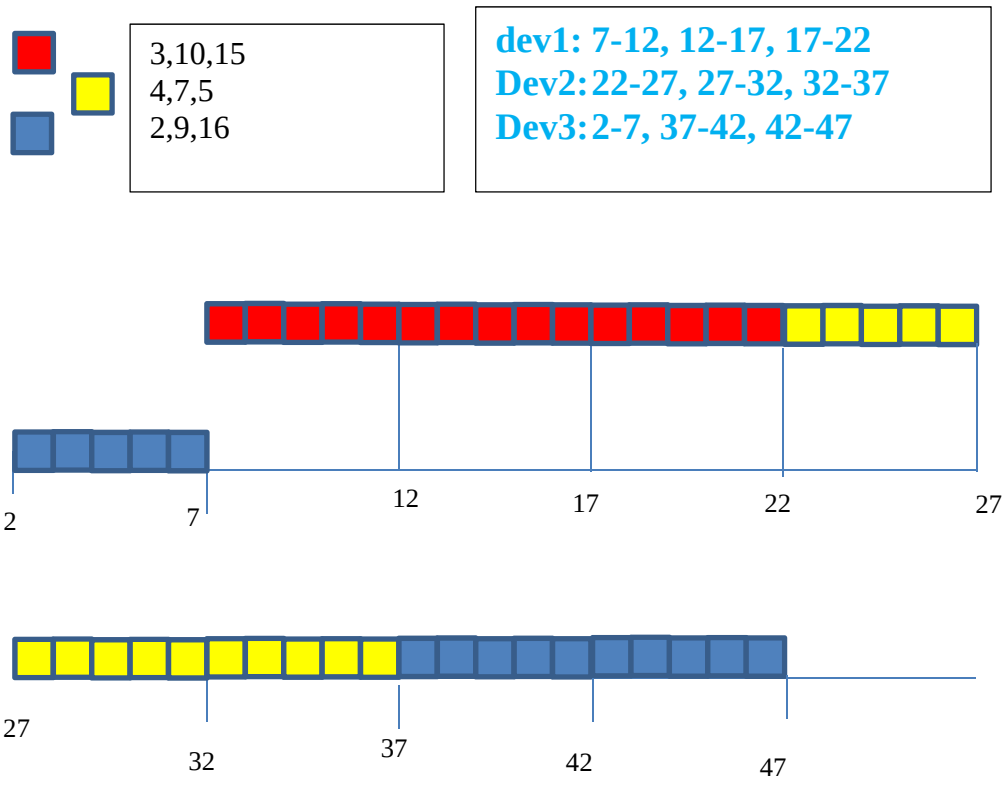
2500 (0x009C4) **000OOOOO1OO11000100 → block 19**

7 (ox00007) **000OOOOOOOOOO0000111 → block 0**

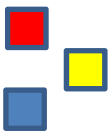
Problem 4 (2+3 points)

Consider 3 devices served by an interrupt based system. The devices are dev1, dev2, and dev3, where dev1 has the highest priority and dev3 the lowest. Each interrupt service routing takes 5 units (ignore context switching).
Devices requested services at the following times
dev1 3,10, 15
dev2 4, 7, 15
dev2 2, 9, 16

a) Assuming no preemption, at what times the three devices are served, put your answer on the form
dev1 from $t_1 \rightarrow t_2$, and $t_4 \rightarrow t_5$



b) Assuming preemption



3,10,15
4,7,15
2,9,16

Dev1: 3-8, 10-15, 15-20
Dev2: 8-10, 20-23, 23-28, 28-33
Dev3: 2-3, 33-37, 37-42, 42-47