EECS 3216
Winter 2021
LAB 1

PULSE WIDTH M0DULATION

Lab Objective

The objective of this lab is to introduce you to Intel-Altera Quartus and Modelsim, and to design and implement a variable duty cycle PWM signal.

Introduction

What is a pulse width modulated signal and its duty cycle?

A PWM signal is a square wave where the percentage of the time the signal is HIGH compared to the cycle time is set to represent some criterion. The percentage of the time the signal is HIGH compared to the cycle time is called the duty cycle. For example, consider the following signal
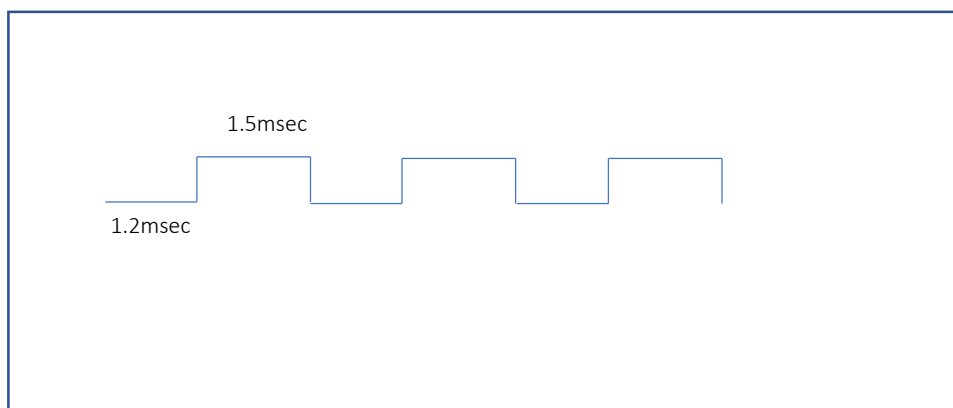
In the square wave shown above, the LOW time is 1.2 msec, and the HIGH part is 1.5 msec. The total cycle time is 2.7 msec. which means the frequency of the PWM is 1/2.7msec = 0.37 KHz or 370 Hz. The duty cycle of the wave is 1.5/2.7 = 55.5%

LAB

Design a circuit to generate a PWM wave with a specific frequency. The duty cycle is determined by the rightmost 3 positional switches on the board. The three positional switches form a binary number from 000(0) -> 111(7).

111 corresponds to a 90% duty cycle

000 corresponds to a 10% duty cycle.

The 80% range is divided equally among the other 6 combinations of the positional switches.

The output is at pin XXX (must check an available pin)

Specifications

1. The PWM frequency is 4 KHz
2. The input is from the 3 right-most positional switches (SW2 SW1 SW0) with SW2 represents the most significant digit
3. The output is sent to LEDR0
4. The input (from the three right-most switches) is displayed on the LEDs (LEDR4 LEDR3 LEDR2) where LEDR4 is the most significant digit (corresponding to SW2)

Deliverables

1. A report containing the following
   a. Your name, student number, and Lab number
   b. Design: How did you reach your implementation. For this lab, you can use English, FSM, tables, or pseudo code. You must specify what will be the duty cycle for all the settings of the switches. You also must explain/show any fixed numbers in your design (A 5-bit counter, why did you choose 5?)
   c. Verilog code
   d. Modelsim simulation results (the waveforms).You must show few settings of the input switches.
2. A video (10 seconds) in the video you show your circuit working and you must change the switches few times to show the change in the display for the output and input

Marking

This lab is worth 1 point (not mark) some labs will be worth 1 point and is doable in 1 week, some labs are worth 2 points and is doable in 2 weeks.

The lab is due 11:59 pm January 27.