Connecting to Coil Arrays

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***Abstract*— A brief discussion on the issue of interfacing chips to pMRI coil arrays.**

I. Introduction

A critical issue for the pMRI integrated receiver designer deals with the issue of actually interfacing to the coil array. How many receivers can an IC house? How many coils can a chip be easily connected to? How will the chip forward its signal to the remaining electronics (e.g. the DSP)? How exactly will the chip be interfaced to the antenna?

II. 2D Circular Coil Array

A. Three Coil Connection

In [1] an array of circular pick-up coils is described. This arrangement is re-drawn in Fig. 1 with a suggestion of where receiver chips (black squares) could be placed to pick up the antenna signals. This picture is scaled such that if the coils have radius of 24-mm, their thickness is 2-mm and the chips are 4-mm on a side. The sizes are inspired by a 90 coil array reported in [2] where 2.5-mm wide, 23-mm coils (radius) were used. The overlap of the coils is suggested in [1] to minimize the coupling between adjacent structures. Another way to place the chips is illustrated in Fig. 2.

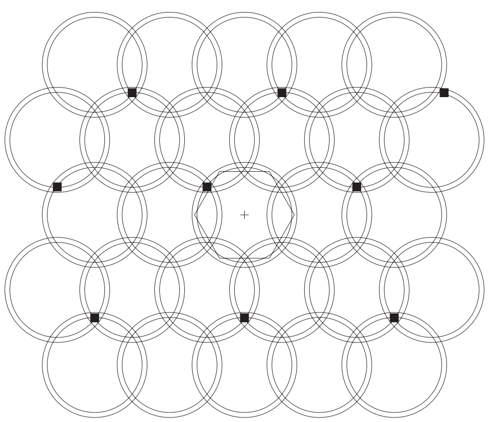

Fig. 1. Chips interfaced to three circular pick-up coils.

As show in Fig. 1 it is possible to place a chip directly on the coil array such that it supports three coils in parallel. The difficulty here lies in the details of how exactly the chip is to be connected to the coils. A close-up view of one possible connection is shown in Fig. 3.

As indicated, small gaps ($\sim 500\ \mu$m) are cut in the coils across which the chip's three receivers are interfaced. The small black dots represent flip-chip solder pumps ($\sim 100\ -\mu$m in diameter). Although conceivable, such a connection may still be infeasible. The overlap region may be highly uneven. As stated in [2] the 90-coil array is built from "from 0.031 inch thick G10 copper clad (1Oz/ft^2) circuit board", this works out to copper lines approximately 34 μm thick on a 787 μm thick dielectric. It is not clear from [2] how exactly the 3-coil overlap region is constructed. For instance, if SMA capacitors are used to couple lines at the intersection area of three coils as shown in Fig. 4. Clearly this type of capacitive bridging of the coil will entirely rule out an central (to the coil intersection) chip connection.

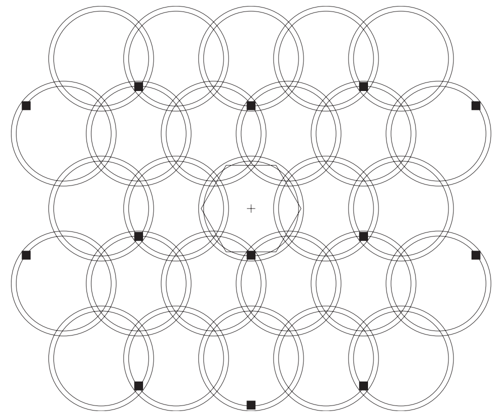

Fig. 2. Another way to interface chips to three circular pick-up coils.

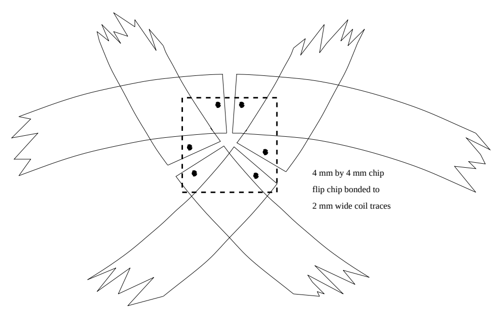

Fig. 3. A close-up view of a chip flip-chip bonded to the ring coils.

Besides the problem of interfacing the chip to the coils, the issue of interfacing the output, supply and ground to this chip. These issues can be alleviated when the three-coil connection shown in Fig. 5. Moving the chips away from the coil intersections leaves a lot more room for the remaining input and output leads that need to be made. One potentially major drawback of this approach is the need for longer leads to connect the chip to three neighboring coils in as symmetric a way as possible. It is possible that these extra leads may interfere somewhat with the intended operation of the pick-up coils.

The simplification of this approach to a two-coil connection is obvious.

Many thanks to the friends of FishLab

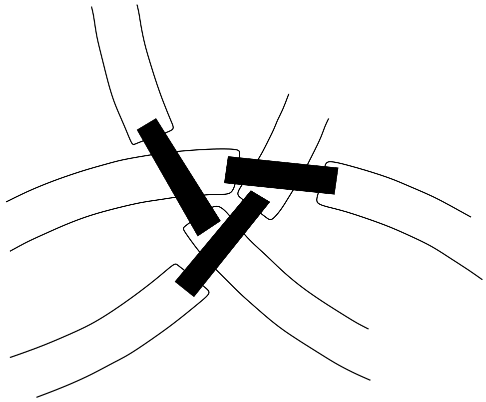

Fig. 4. A close-up view of the possible intersection of three coils. The coils are shown bridged by SMA capacitors.

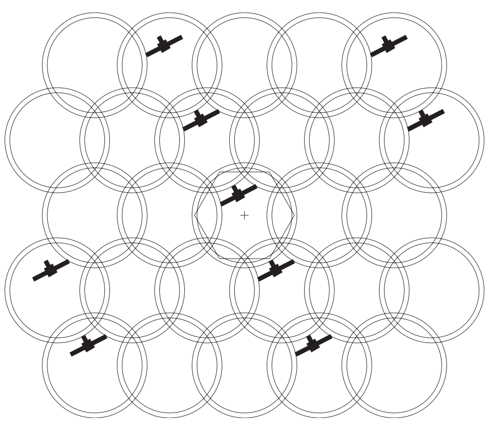

Fig. 5. Another way to interface chips to three circular pick-up coils with more room for output, power, and ground connections.

B. Four Coil Connection

Another possible chip-to-coil connection arrangement is shown in Fig. 6. In this case we imagine the chips placed such that they are in proximity to four coils.

One possible way of interfacing the chip to the coils is shown in Fig. 7. Although two of the coils require longer path connections (thus introducing some asymmetry) the chip to coil connection does not have to directly deal with the SMA capacitor bridges.

Fig. 7 also suggests the possible power supply, ground, and output connections to the chip. The outputs from the four parallel receivers are placed at the four corners of each chip and connected out to small copper pads to which connections may be soldered. The mechanical integrity of such a connection is questionable however. The power supply and ground can be supplied through the back of the substrate; the unlabelled dark connections on the chip in Fig. 7 indicate flip-chip bonds to (board) through-holes connecting out to power and ground connections (not shown).

III. Planar Rectangular Coil Array

In [3] a planar rectangular coil array is described. An illustration of three adjacent coils in this array is given in Fig. 8. This particular design is intended for a 4.7-T MRI machine and the array fabricated in [3] consisted of 64 coils.

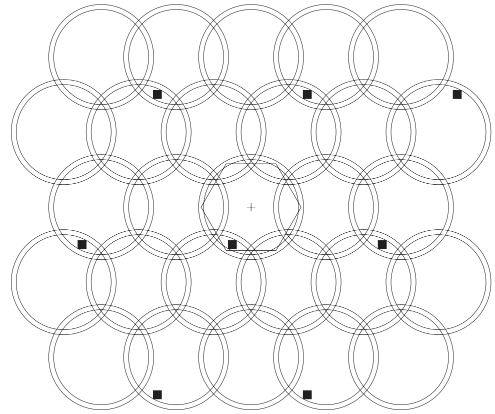

Fig. 6. Chips interfaced to four circular pick-up coils.

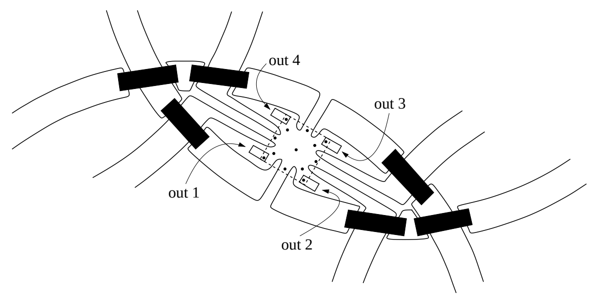

Fig. 7. A close-up view of the possible interface of a chip to four pick-up coils. SMA capacitor connections are also shown.

In this design, the footprint of each coil (including intercoil spacing) is 2.032 mm. Thus, 64 coils extend over a length of 13 cm.

Also shown in Fig. 8 is the manner in which the receiver is electrically attached to a coil. Varactor diodes, D_1 and D_2 are used to tune the coil to the correct central operating frequency. The diodes are shown separately in the picture, but it may be possible to integrated these directly (ideally, as MOS varactors) alongside the receiver IC bonded to the coil.

A more in-depth sketch of the electrical connectivity of a channel in the 64-coil 4.7-T design of [3] is shown in Fig. 9. An ideal integrated front-end would be capable or replacing all the components following the 1-nF DC blocking capacitor.

A possible way to interface the integrated receiver (along

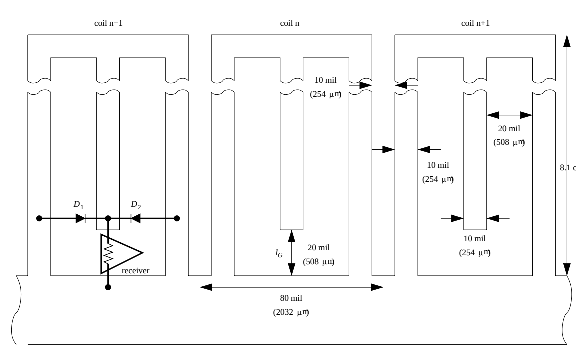

Fig. 8. Three coils from the 64 coil 4.7-T array described in [3].

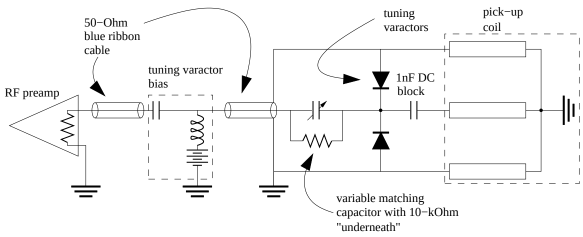

Fig. 9. The connection details (to the preamp) for each channel of the 64-coil 4.7-T array in [3].

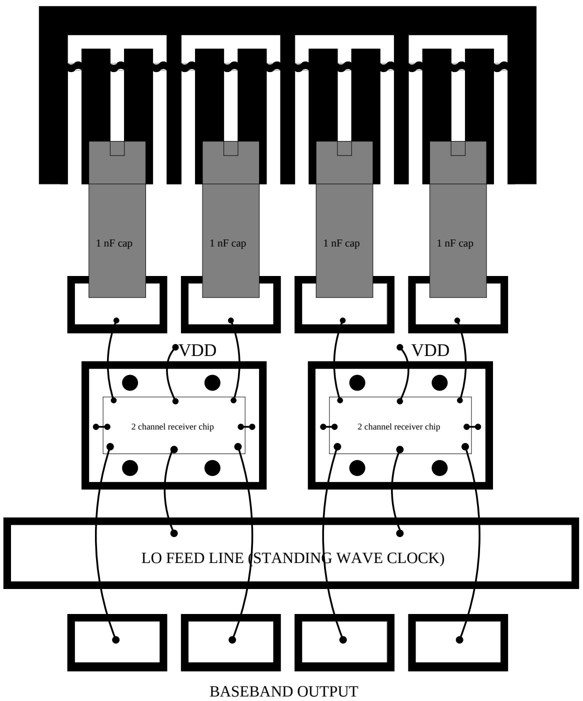

Fig. 10. Possible receiver board-level attachment to the coil array.

with on-chip tuning diodes) is shown in Fig. 10. Note still the absence of any current bias and varactor tuning nodes. Under the current drawing this is difficult. The only immediate space where in pins may be located to these ports are in between the chips in the layout shown. This is highly confining, as the spacing between the ground planes (the board cut-outs on which the chips are placed) is only around 20 mil.

A simple way to open more room for contacts is to re-orient the chips by 90° as shown in Fig. 11. This opens some room for five reasonably sized pads (60 mil by 30 mil or 1.524 mm by 0.762 mm) to which external wired connections can be made (to another board). This only leaves 2.5 connections per channel (since each chip contains two channels). With the need for two tuning voltages and at least two bias controls per chip this is clearly not enough. But if the long dimensions of the periphery pads can be halved we can make available five external connections per channel. This may be just enough.

For the 64-coil array, which altogether spans 13 cm we can, as done in [3] stretch the pitch of the connections from 2 mm to approximately 2.5 mm by proper routing from coils to chips. This gives us about a 20% 1D increase and with small pad sizes could now allow 6 connections per channel. Of

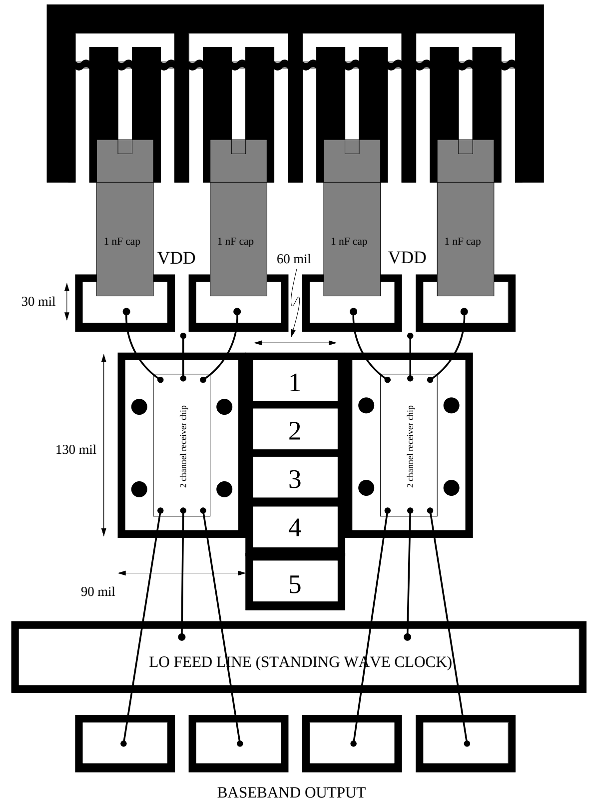

Fig. 11. Another possible receiver board-level attachment to the coil array.

course this approach extends the net extend of the electronics attached to the array to 16 cm in the case of the 4.7-T 64-coil array. Such an approach is obviously limited by the size of the magnet bore (18-cm in the case of the studies reported in [3]).

References

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[3] M. P. McDougall, *Single Echo Acquisition Magnetic Resonance Imaging*, Ph.d. dissertation, Texas A&M University, December 2004.