Common-Source LNA: Gain

Sebastian Magierowski

***Abstract*— A brief discussion of the suitability of the common-source 0.18-μm NMOS LNA for the 200-MHz 4.7-T MRI receiver under consideration. Only the gain properties are discussed.**

I. Introduction

The cascoded common-source (CS) LNA has become the workhorse of narrowband integrated receivers. Considering a 0.18 μm CMOS technology, how will it fare in our 200-MHz MRI application? This note is a preliminary and not overly rigorous discussion of this issue. It is hoped that it raises enough points to inspire more rigorous insights in future. Only the issue of amplifier gain is discussed in this note.

II. Knowns

Unfortunately, nothing is completely fixed in the project at this point, but Dr. Wright has noted that in previous experiments the source (i.e. pick-up coil) has been modelled with a series RL circuit as shown in Fig. 1 having a Q of

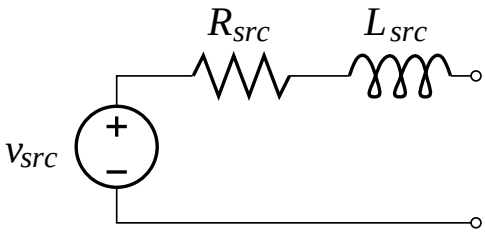

Fig. 1. Series RL model of pick-up coil.

about 40 and a reactance of about 71 Ω. Thus, at 200-MHz the series source resistance is

$$R_{src} = \frac{X_{src}}{Q} = \frac{71}{40} = 1.78\ \Omega. \tag{1}$$

. The series inductance of the source is

$$L_{src} = \frac{X_{src}}{\omega_0} = \frac{71}{2\pi 200 \times 10^6} = 56.5\ \text{nH}. \tag{2}$$

Assuming that these are indeed the pick-up coils we will use (which is perhaps not really all that certain) our space of "given" now ends and the remainder is a sea of design variables.

III. LNA Driving Point Characteristics

To start our survey of the design space we consider the input impedance of the NMOS LNA (i.e. its driving point characteristics). Throughout we will assume that NMOS FETs with a 0.18-μm channel length (drawn) are used. If the

Many thanks to the friends of FishLab

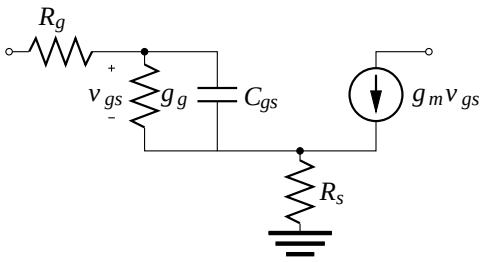

Fig. 2. Small-signal circuit equivalent of cascode CS LNA.

on/effective/overdrive voltage $V_{on} = V_{GS} - V_t$ is not too big[1] choosing a minimum channel length is necessary to minimize thermal noise (because electrons take less time to get through the device and therefore experience less "randomizing collisions" during transport).

With the channel length set, two fundamental FET parameters remain — the total effective width, W_{eff}, and the biasing on voltage (again), V_{on}. The specific device-type that we will consider is the deep n-well (DNW) NMOS intended specifically for RF applications (although 200-MHz is not really pushing the RF aspect in comparison to present-day consumer applications). The technology is assumed to be TSMC's 0.18-μm mixed-mode CMOS process. The model name typically used in the Cadence TSMCp18 kit for this device is `nmos_rf`. The DNW RF transistor can consist of 1 to 64 gate fingers with the allowable width of each finger ranging between 1.5 to 8 μm.

The small-signal model of the CS LNA is shown in Fig. 2. The input impedance of this circuit is given by

$$Z_{in}(\omega) = R_g + R_s + \frac{(1 + g_m R_s)}{g_g + j\omega C_{gs}} \tag{3}$$

where R_g is the polysilicon gate resistance, R_s is the extrinsic (MOSFET) source resistance (not to be confused with the pick-up coil source resistance R_{src}), g_m is the device transconductance, g_g is the channel-induced gate conductance and C_{gs} is the gate-to-source capacitance. Because we are considering a cascode configuration C_{gd} is ignored.

A useful expression for the transconductance is [1]

$$g_m = \mu_{eff} C_{ox} \frac{W_{eff}}{L_{eff}} \alpha V_{on} \tag{4}$$

where C_{ox} is the oxide capacitance per unit gate area and where α is [2]

$$\alpha \equiv \frac{g_m}{g_{do}} = \frac{1 + \rho/2}{(1+\rho)^2} \tag{5}$$

[1] Don't ask me what "too big" is at this point, I do not know.

in which g_{do} is the MOSFET channel conductance when $V_{DS} = 0$ and

$$\rho = \frac{V_{on}}{L_{eff} E_{sat}} \tag{6}$$

where E_{sat} is the field strength at which the carrier velocity is half the value extrapolated from low-field mobility measurements [3]. It is typically taken around 4×10^4 V/cm.

There are a number of ways to express the effective mobility. For the time being we employ [1]

$$\mu_{eff} = \frac{v_{sat}}{E_{sat}/2} \tag{7}$$

where v_{sat} is the maximum electron drift velocity attainable in the channel. Given the low-field dependence between drift velocity, mobility, and electric field (i.e. $v_d = \mu E$), this expression follows from the definition for E_{sat} given above.

The total value of the capacitance between the gate-source terminals of the device is given by

$$C_{gs} = \frac{2}{3} W_{eff} L_{eff} C_{ox} + C_{gs,m} \tag{8}$$

where $C_{gs,m}$ is the extrinsic capacitance contributed by local metal interconnect around the transistor. For a single minimum length stripe 5-μm in width the total gate-source saturation capacitance predicted by the above equation is around 6.3-fF (of which 1.8 fF is due to the metal interconnect) and rises (linearly) to 306-fF (of which 18.4 fF is due to the metal interconnect) for a 64-strip transistor.

The extrinsic resistance, R_s can be calculated based on the source area, number of finger, number of contacts as well as interconnect metal conductivity. For a MOSFET with 5-μm unit (i.e. finger) width, R_s is around 1.4 Ω for a 1-finger device and 0.45 Ω for a 64-finger device bottoming out at about 0.36-Ω for 30 fingers.

The polysilicon gate resistance, R_g, is a critical variable that can dominate the real part of the impedance seen looking into the LNA. A worthwhile approximation to this is [1]

$$R_g = R_{sh} \frac{W_{eff}}{12 n^2 L_{eff}} + \frac{R_{con}}{W_{eff} L_{eff}} \tag{9}$$

where R_{sh} is the sheet resistance of the silicided gate material (reasonably 10 Ω/sq [1]), R_{con} is the silicide-to-poly contact resistance and runs about 25 $\Omega \cdot \mu$m^2 [1], The n denotes the number of fingers used in the layout. This expression predicts a gate resistance of 57 Ω for a single 0.18-μm finger of 5-μm width; for 32 fingers it predicts 1.8 Ω and for the full 64-finger complement it predicts 0.9 Ω.

The expression for g_g is

$$g_g = \frac{\omega^2 C_{gs}^2}{5 g_{do}} \tag{10}$$

This value obviously depends on the frequency of operation, the size of the device as well as biasing. However, to get a feel for the magnitude, at 200 MHz, $V_{on} = 200$ mV, $W_u = 5$ μm, and one (minimum length) finger $1/g_g = 210$ MΩ. For a 64-finger device this drops to 5.7 MΩ. Increasing V_{on} increases $1/g_g$.

We lump all of the above characteristics into a simple parallel RC circuit equivalent for the input impedance of the LNA. The parallel equivalent resistance is a function of both W_{eff} and V_{on} and is plotted in Fig. 3. In this plot we actually consider a "device" consisting of four transistors (each with the same number of fingers) attached in parallel (hence the $N_d = 4$ label). This is necessary for large devices as design rules prevent us from building DNW FETs with more than 64 fingers. As noted each finger's unit width, W_u, is 5 μm.

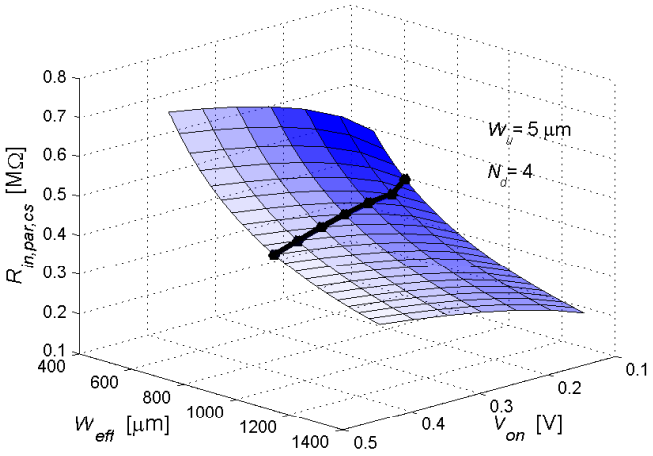

Fig. 3. Parallel equivalent input resistance of 0.18-μm common-source cascode LNA. The solid black line denotes 0.4-MΩ.

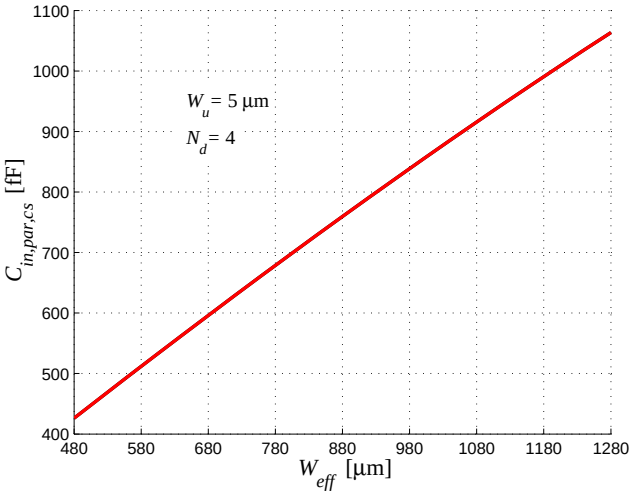

Fig. 4. Parallel equivalent input capacitance of 0.18-μm common-source cascode LNA.

The equivalent parallel input capacitance is essentially equivalent to C_{gs} which is only dependent on the net device width. This is plotted in Fig. 4.

Since the driving point impedance of the cascode CS LNA (at 200-MHz) is dependent on the size and bias of the device we have ample room to vary the circuit characteristics. As a representative example we can consider the device (remember by "device" we are actually thinking of four separate layouts strung together) with $W_{eff} = 840$ μm and $V_{on} = 250$ mV (this is entirely an arbitrary choice, without any particular insight on the part of the author). For this device the our

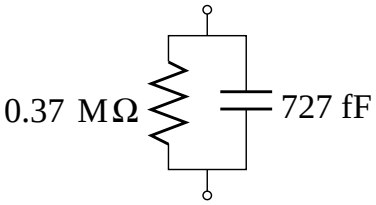

Fig. 5. Parallel equivalent RC circuit model for CS cascode LNA input with $W_{eff} = 840$ μm and $V_{on} = 250$ mV.

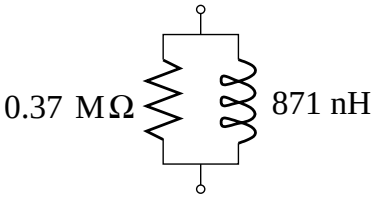

Fig. 6. Parallel equivalent RL circuit model for the source impedance transformed by the matching network for a CS cascode LNA with $W_{eff} = 840$ μm and $V_{on} = 250$ mV operating at 200 MHz.

equivalent input impedance is as drawn in Fig. 5.

IV. Gain Characteristics

The data accumulated so far on the signal source and the amplifying transistor is great news as far as the gain is concerned. Why is that? Is it because we have a source capable of delivering a great deal of power (because R_{src} is low) and a load which requires very little power (because $R_{in,par,cs} = R_l$ is high, ~ 0.37 MΩ).

Placing a proper matching network between such a source and such a load results in a voltage gain (from source to amplifier input) of [2]

$$\frac{v_l}{v_{src}} = \frac{1}{2}\sqrt{\frac{R_l}{R_{src}}} \sim \frac{1}{2}\sqrt{\frac{0.37 \times 10^6}{1.7}} = 47 \text{ dB}. \tag{11}$$

where v_l is the voltage drop from between the gate terminal of the LNA and ground. Any of a number of matching circuits could facilitate this. The matching circuit in this case transforms the source impedance to the parallel RL equivalent drawn in Fig. 6.

The net transconductance gain of the LNA then becomes

$$\begin{aligned} G_m &= g_m \cdot \frac{v_{gs}}{v_{src}} = g_m \cdot \frac{v_{gs}}{v_l}\frac{v_l}{v_{src}} \\ &= g_m \left|\frac{Z_{gs}}{Z_{in}}\right| \frac{1}{2}\sqrt{\frac{R_l}{R_{src}}} \end{aligned} \tag{12}$$

where

$$Z_{gs} = \frac{1}{g_g + j\omega C_{gs}}. \tag{13}$$

With $g_m = 278.3$ mS for the device under consideration (i.e. $W_{eff} = 840$ μm, $V_{on} = 250$ mV) and $|Z_{gs}/Z_{in}| = 0.9$ our transconductance gain is $G_m = 35$ dB.

And what's the cost of this gain? Using the following expression for the drain current [1]

$$I_D = \frac{C_{ox} v_{sat} W_{eff} V_{on}^2}{V_{on} + L_{eff} E_{sat}} \tag{14}$$

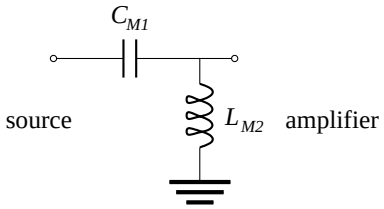

Fig. 7. Gain matching network B (GMB).

we find that our middle-of-the-road (maybe) device draws a hefty 40 mA, for a total of 72 mW drawn from a 1.8-V supply.

Is all this (gain, power, size, etc.) any good? It depends on a detailed examination of the remaining RF stages which will be the subject of future (of the immediate variety) work. For now it seems that we should be able to lower the current substantially and still operate at a decent gain, 20 dB say.

To get a stronger feel for this we do some number crunching. First we consider a specific gain matching network between the pick-up coil and the amplifier. We only look at the very simple L-match network shown in Fig. 7 (for our own personal historical reference we will refer to this matching network as — GMB — gain match network B). We choose this network because it provides reasonable component values (shielded 300-nH inductors are readily available) and the series capacitance can double as a DC blocker.

The component values of the matching network over various LNA device variables are shown in Fig. 8. Over a rather wide set of device operating parameters the C_{M1} varies between about 0.7 and 1.2 pF. Such values may even be sustainable on-chip without extravagant stress on area. The shunt inductance, L_{M1}, varies between about 300 and 500-nH. As mentioned above, compact, shielded components should readily be available in this range (variability is another matter however).

The transducer gain, $G_{m,GMB}$ under GMB is as shown in Fig. 9. As shown (the dark line denotes values at 32 dB), high gains are relatively easy to obtain (again, how useful these transconductance "gains" are depends on the mixer that loads the amplifier) and that we have a lot of room to lower the power consumption.

For instance, with $W_{eff} = 840$ μm and $V_{on} = 100$ mV we still get a transconductance around 28-dB, but, looking at Fig. 10, draw only 7.7-mA of dc drain current, I_D.

References

[1] L. Belostotski, "Personal communication," June 2007.
[2] D. G.-W. Yee, *A Design Methodology for Highly-Integrated Low-Power Receivers for Wireless Communications*, Ph.d. dissertation, University of California, Berkeley, Spring 2001.
[3] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, Cambridge, 2nd edition, 2004.

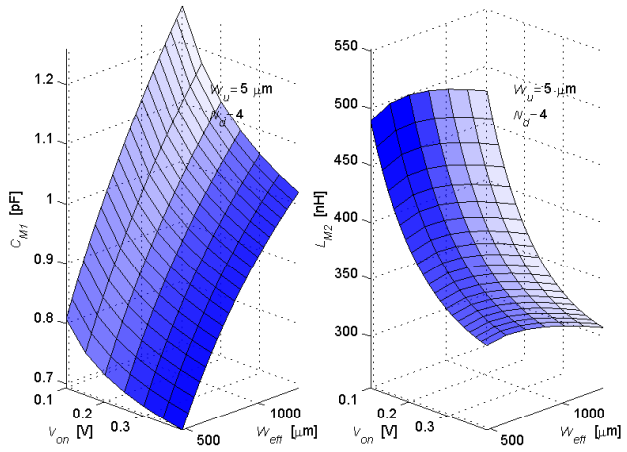

Fig. 8. Simple matching network components for optimal power gain.

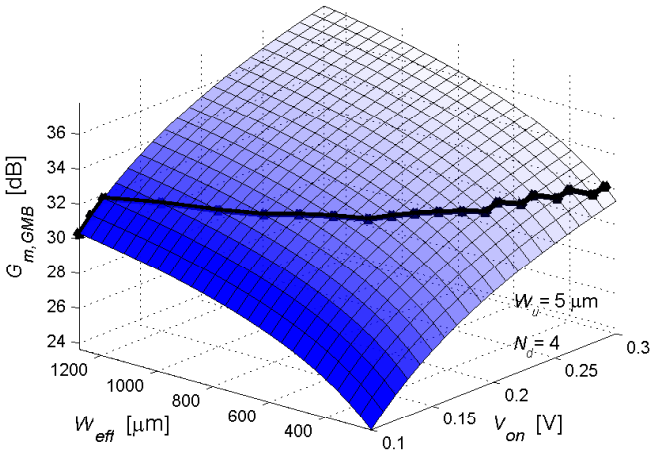

Fig. 9. The transconductance for a cascode CS LNA with matching network B between it at the pick-up coil. The thick line denotes transconductance gains of 32-dB.

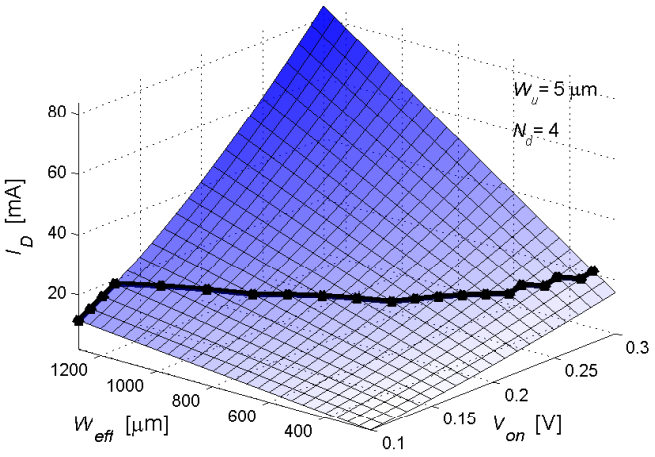

Fig. 10. The drain bias current drawn by a cascode CS LNA. The thick line denotes currents of 20 mA.