Common-Source LNA: Noise

Sebastian Magierowski

Abstract— A brief discussion of the suitability of the commonsource 0.18-μm NMOS LNA for the 200-MHz 4.7-T MRI receiver under consideration from a noise performance perspective.

I. INTRODUCTION

In an earlier technical note [1] we discussed the gain characteristics of the common-source (CS) cascode LNA built out of a 0.18- μ m CMOS technology for a 200-MHz MRI receiver. In this technical note we continue our investigation of this circuit, but now focus on the "n"-word: noise.

II. NOISE BACKGROUND

The expression for the noise factor of a CS LNA (assumed cascode so C_{gd} can be ignored) is [2] (note: the same expression can be used for the common-gate LNA)

$$F_{eqn} = 1 + \frac{\alpha \delta \omega^2 C_{gs}^2}{5g_m G_s} + \frac{\gamma}{\alpha g_m G_s} \left[(g_g + G_s)^2 + (\omega C_{gs} + B_s)^2 \right] + 2|c| \sqrt{\frac{\delta \gamma}{5}} \frac{\omega C_{gs}}{g_m G_s} (\omega C_{gs} + B_s).$$
(1)

The variables, α , ω , C_{gs} , g_m , and g_g have already been discussed in [1]. The terms G_s and B_s are simply the conductance and susceptance of the parallel equivalent source impedance seen by the LNA. In [1] we started the whole analysis from the assumption that our source consists of a 1.7- Ω resistance in series with a 56-nH inductance. The parallel equivalent of this circuit at 200-MHz is shown in Fig. 1.



Fig. 1. Parallel equivalent input impedance of our assumed input coil at 200 MHz.

The remaining terms: γ , δ , and c pertain to the noise behaviour of the LNA's transistor. We will not labor on the details of these parameters, they are adequately discussed in [3]. However, given the prodigious amount of ink spilled on discussions of these parameters it seems only sensible to explore them a little.

 γ keeps track of the thermal noise associated with the MOSFET's channel. For long-channel devices in saturation

this value is 2/3 reflecting the tapered shape of the saturated FET's channel (this is the same reason that we often express $C_{gs} \propto 2C_{ox}/3$). For over two-decades now, the rapid scaling of MOS technology into the sub-micron regime has inspired researches to re-visit time-and-again the value of γ . In [4] Abidi reported values ranging from 1.6 to 8. Likely he was lumping a number of effects into the γ term (he used rather high bias voltages). The work of Scholten et al. [5] is a highly regarded contribution to the work. Therein, γ values between 2/3 and unity were reported for 0.18- μ m CMOS transistors. It seems that in general, the long channel theory still holds for short-channel devices at reasonable biasing and deviations from this value may be attributable to extrinsic components (such as MOSFET source resistances) [6]. Thus, in this note we will follow classical long-channel dictates and assume that $\gamma = 2/3.$

Similarly, we will retain $\delta = 4/3$, another result which follows from classical long-channel approximations. Is another weighting factor dependent on the shape of the MOSFET channel. A nice, tapered channel like the one we observe in saturation of long-channel devices results in the 4/3 value.

At last, the parameter c denotes the correlation between the channel thermal noise caused by irregular motions in the channel and the channel-induced gate noise caused by the same irregular motions in the channel. Once again, we will resort to the long-channel results which is c = j0.395.

A. F derivation

How is the equation for F_{CS} shown above derived? In a simple but tedious manner. Any of a number of references go into suitable detail on this [2], [3], but, in a nutshell, all we have to do is find the current at the output due to the driving source, i_{osrc} , as well as all noise sources associated with the transistor, i_{ofet} and calculate the following

$$F = \frac{\operatorname{var}[i_{oscr} + i_{ofet}]}{\operatorname{var}[i_{oscr}]} \tag{2}$$

where "var" denotes the variance operation. Assuming that the source noise is not at all correlated with the device noise we have

$$F = 1 + \frac{\operatorname{var}[i_{ofet}]}{\operatorname{var}[i_{oscr}]}.$$
(3)

Equation (1) was derived in this way for a CS LNA with the small-signal model illustrated in [2] (Fig. 6.9, pg. 147). For the sake of completeness however, we would like to find an expression for F that is in-line with a more accurate (small-signal) model of the transistor. This model was discussed in [1] and is shown again in Fig. 2 for convenience.

Many thanks to the friends of FishLab



Fig. 2. Small-signal circuit equivalent of cascode CS LNA.



Fig. 3. Small-signal circuit equivalent of cascode CS LNA with noise sources.

III. NOISE FOREGROUND

In deriving an expression for the noise factor for the amplifier model of Fig. 2 we must consider five noise sources (all thermal in nature) in total:

- *i*_{src} the current noise of the driving source (i.e. the pickup coil).
- 2) i_d the current noise of the channel.
- 3) i_{dg} the channel current noise that's induced in the gate of the transistor.
- 4) i_{rq} the current noise of the polysilicon gate resistance.
- 5) i_s the current noise of the source resistance.

Fig. 3 is a sketch of the CS LNA along with the intrinsic noise sources (i.e. i_{src} is not included in the sketch).

In deriving Eq. (1) only the first three noise terms were used. Also, as seen in Eq. (3) to calculate the noise factor we must find the current contributed at the output of the device by each of the noise sources. That is, our noise factor calculation actually comprises

$$F_{brute} = 1 + \frac{\operatorname{var}[i_{od} + i_{odg} + i_{org} + i_{os}]}{\operatorname{var}[i_{oscr}]}$$
(4)

where the "o" has been added to the subscript labels to denote that the output current noise contributions are being considered. Perhaps a more familiar expression of the above equation is

$$F_{brute} = 1 + \frac{\overline{i_{od}^2} + \overline{i_{odg}^2} + \overline{i_{org}^2} + \overline{i_{os}^2} + \overline{i_{odg}}i_{od}^* + \overline{i_{odg}^*i_{od}}}{\overline{i_{osrc}^2}}.$$
(5)

Let us find expressions for each of these terms.

A. Drain Noise

The output drain current noise density is simple (for conciseness we will ignore the Δf term typically included with these expressions).

$$\overline{i_{od}^2} = 4kT\gamma g_{do}.$$
(6)



Fig. 4. Small-signal circuit with R_s absorbed.

B. Induced Gate Noise

To find $\overline{i_{odg}^2}$ we must first find how much induced gate noise current appears back at the drain output. Elementary circuit theory guides us here. Consider the circuit in Fig. 4. This is equivalent to the model in Fig. 2, but with the source resistance absorbed in g'_m and Z_{in2} . Specifically,

$$g'_m = \frac{g_m}{1 + g_m R_s} \tag{7}$$

and

$$Z_{in2} = \frac{1}{Y_{in2}} = R_s + Z_{in1}(1 + g_m R_s)$$
(8)

where

$$Z_{in1} = \frac{1}{Y_{in1}} = \frac{1}{g_g + j\omega C_{gs}}.$$
(9)

A little KCL (on the circuit shown in Fig. 3 with all noise sources but i_{dq} removed) shows that

$$i_{odg} = \frac{Z_{in2}(R_g + Z_{src})g'_m i_{dg}}{Z_{in2} + R_g + Z_{src}}.$$
 (10)

A bit more tidying up gives

$$i_{odg} = \frac{g'_m i_{dg}}{\frac{1}{R_g + Z_{src}} + \frac{1}{Z_{in2}}}.$$
 (11)

Defining

we reach

$$Y_{src2} = \frac{1}{R_g + Z_{src}} \tag{12}$$

i _ $g'_m i_{dg}$

$$i_{odg} = \frac{g_m \iota_{dg}}{Y_{src2} + Y_{in2}}.$$
 (13)

Finally,

$$\overline{i_{odg}^2} = \frac{(g'_m)^2 \overline{i_{dg}^2}}{(\text{Re}\{Y_{src2} + Y_{in2}\})^2 + (\text{Im}\{Y_{src2} + Y_{in2}\})^2} \quad (14)$$

where

$$\overline{j_{dg}^2} = 4kT\delta g_g. \tag{15}$$

C. Resistive Gate Noise

We can resort to the same model as in Fig. 4 when looking to calculate $\overline{i_{org}^2}$. Another helping of KCL (on the circuit shown in Fig. 3 with all noise sources but i_{rg} removed) produces

$$i_{org} = \frac{Z_{in2}R_g g'_m i_{rg}}{Z_{in2} + R_g - Z_{src}}.$$
 (16)

Rearranging gets us to

$$i_{org} = \frac{g'_m i_{rg}}{\frac{1}{Z_{in2}} + \frac{1}{R_g} - \frac{1}{R_g} \frac{Z_{src}}{Z_{in2}}},$$
(17)

which can be compressed to

$$i_{org} = \frac{g'_m i_{rg}}{Y_{in2} + G_g (1 - Y_{in2}/Y_{src})}$$
(18)

where $G_g = 1/R_g$. Finally,

$$\overline{i_{org}^2} = \frac{(g'_m)^2 i_{rg}^2}{(\operatorname{Re}\{Y_{in2} + G_g(1 - \frac{Y_{in2}}{Y_{src}})\})^2 + (\operatorname{Im}\{Y_{in2} - \frac{G_g Y_{in2}}{Y_{src}}\})^2}$$
(19)

where

$$\overline{i_{rg}^2} = 4kTG_g.$$
(20)

D. MOSFET Source Resistance Noise

Working with the small-signal model first presented and shown in Fig. 3 (with all noise sources but i_{rg} removed) we can show that

$$i_{os} = \frac{R_s Z_{in1} g_m i_s}{R_g + R_s + Z_{in1} (1 + g_m R_s) + Z_{src}}.$$
 (21)

Rearranging we arrive at

$$i_{os} = \frac{R_s g_m i_s}{(Z_{src} + Z_{in})/Z_{in1}}.$$
 (22)

where, as shown in [1],

$$Z_{in} = R_g + Z_{in2}. (23)$$

Finally, we have

$$\overline{i_{os}^2} = \frac{g_m^2 R_s^2 i_s^2}{(\operatorname{Re}\{Z_{src} + Z_{in})/Z_{in1}\})^2 + (\operatorname{Im}\{Z_{src} + Z_{in})/Z_{in1}\})^2} \tag{24}$$

where

$$\overline{i_s^2} = 4kTG_s \tag{25}$$

in which $G_s = 1/R_s$.

E. MOSFET Cross-Correlation Noise

Now, referring to Eq. (13) we have for $\overline{i_{odg}i_{od}^*}$

$$\overline{i_{odg}i_{od}^*} = \frac{g'_m \overline{i_{dg}i_{od}^*}}{Y_{src2} + Y_{in2}}.$$
(26)

From [2]

$$\overline{i_{dg}i_{od}^*} = (\overline{i_{dg}^*i_{od}})^* = c\sqrt{\overline{i_{dg}i_{dg}^*} \times \overline{i_{od}i_{od}^*}} = j|c|\sqrt{\overline{i_{dg}i_{dg}^*} \times \overline{i_{od}i_{od}^*}}$$
(27)

therefore

$$\overline{i_{odg}i_{od}^*} = \frac{g'_m j |c| \sqrt{i_{dg}^2} \ \overline{i_{od}^2}}{Y_{src2} + Y_{in2}}.$$
(28)

Similarly,

$$\overline{i_{odg}^{*}i_{od}} = \frac{g'_{m}i_{dg}^{*}i_{od}}{(Y_{src2} + Y_{in2})^{*}}$$
(29)

which is

$$\overline{i_{odg}^* i_{od}} = -\frac{g'_m j |c| \sqrt{i_{dg}^2 i_{od}^2}}{(Y_{src2} + Y_{in2})^*}.$$
(30)



Fig. 5. Small-signal CS LNA circuit with source noise.



Fig. 6. Parallel equivalent RL circuit model for the source impedance required for optimum noise match to a CS cascode LNA with $W_{eff} = 840 \ \mu m$ and $V_{on} = 250 \ mV$ operating at 200 MHz.

F. Source Noise

Referring to Fig. 5, the output noise current due to the source is

$$i_{osrc} = \frac{g'_m i_{src}}{Y_{in2} + Y_{src}(1 + Y_{in2}R_g)} = \frac{g'_m i_{src}}{Y_{sden}}.$$
 (31)

Hence,

$$\overline{i_{osrc}^2} = \frac{(g'_m)^2 i_{src}^2}{(\text{Re}\{Y_{sden}\})^2 + (\text{Im}\{Y_{sden}\})^2}$$
(32)

IV. DESIGN CONSIDERATIONS

A. Feeling out the Design Space

According to Yee [2] the source conductance and susceptance needed to minimize the noise figure in the CS LNA are

$$G_{opt} = \sqrt{\frac{\alpha^2 \delta (1 - |c|^2) \omega^2 C_{gs}^2}{5\gamma}}$$
(33)

and

$$B_{opt} = -\omega C_{gs} \left[1 + \alpha |c| \sqrt{\frac{\delta}{5\gamma}} \right]. \tag{34}$$

For a device with and effective width of $W_{eff} = 840 \ \mu m$ and $V_{on} = 250 \ mV$ the optimal (parallel equivalent) source impedance predicted is as shown in Fig. 6

With such a noise source, the noise figure as predicted by the simplified Eq. 1 is as shown in Fig. 6. In the plot the terms R_{src} and L_{src} refer to the series equivalent RL representation of the source feeding the circuit. At $W_{eff} = 840 \ \mu\text{m}$ and $V_{on} = 250 \ \text{mV}$ the predicted noise figure is 0.01165 dB. Repeating the calculation but this time using Eq. (5) results in the NF plotted in Fig. 8. This calculation predicts a noise figure of 0.02131 dB for $W_{eff} = 840 \ \mu\text{m}$ and $V_{on} = 250 \ \text{mV}$.

Clearly, we can attain extremely good noise behaviour when the optimal source impedance is used. What happens when we consider different source impedances? What values should we consider? If a good gain is one over our objectives, we should consider the noise performance as the parallel equivalent



Fig. 7. The NF as calculated using Eq. (1) when the generator source impedance is set to the value shown in Fig. 6.



Fig. 8. The NF as calculated using Eq. (5) when the generator source impedance is set to the value shown in Fig. 6.

source resistance, $R_{src,p}$ is increased. Recall from Fig. 6 that an optimal source appears with $R_{src,p} = 2826 \ \Omega$.

Now, if we were to use a matching network to convert our actual source impedance (series-equivalent $R_{src} = 1.7 \Omega$) into the optimal source impedance for noise performance we would be sacrificing about

$$10\log\left(\frac{0.37\times10^6}{2.826\times10^3}\right) = 22 \text{ dB}$$
(35)

of gain. Rather than getting roughly 35-dB of (transconductive) gain, we are down to about 13 dB. This is not awful, but we can probably do better with just a marginal sacrifice in noise performance.

So, how bad does the noise performance get when we increase $R_{src,p}$. A comparison is shown in Fig. 9 for values of 10 k Ω , 50 k Ω , and 100 k Ω . Two things are obvious, one, the NF gets worse and two, it becomes more strongly dependent on the device width.



Fig. 9. NF comparison for sources with different parallel equivalent source resistances, $R_{src,p}$ (see legend) and inductance $L_{src,p} = 712.9$ nH.

Still, the degradation in NF is fairly tolerable and the width dependence is a minor penalty, we simply set the design to the optimal width. Table I summarizes the achievable noise performance around the troughs of the results shown in Fig. 9 (a $W_{eff} = 840 \ \mu m$ is selected) at various values of V_{on} .

TABLE I NOISE FIGURE FROM FIG. 9 AT $W_{eff} = 840~\mu m$ and $L_{src,p} = 712.9~nH$

-		
$R_{src,p}$	V_{on}	NF
$[k\Omega]$	[mV]	[dB]
	100	0.072
	150	0.056
10	200	0.049
	250	0.045
	100	0.333
	150	0.261
50	200	0.227
	250	0.209
	100	0.641
	150	0.506
100	200	0.442
	250	0.407

Now, what about changes in $L_{src,p}$? The chances in noise figure as $L_{src,p}$ takes on values of 500, 700, and 900 nH (while $R_{src,p} = 100 \text{ k}\Omega$) are shown in Fig. 10. Now, three main characteristics are observable. One, as with increases in $R_{scr,p}$, increasing $L_{src,p}$ makes the NF more dependent on device width. Two, the best achievable NF clearly improves as $L_{src,p}$ is increased. Three, the device W_{eff} at which the optimal NF is realized decreases as $L_{src,p}$ increases.

Table II summarizes the achievable noise performance around the troughs of the results shown in Fig. 10 at various values of V_{on} .

So, we see that at least up to 900 nH, increasing the effective inductance (i.e. transformed by some matching network) is a tremendous advantage, that not only improves the noise performance but decreases the device width at which the



Fig. 10. NF comparison for sources with different parallel equivalent source inductances, $L_{src,p}$ (see legend) and resistance $R_{src,p} = 100 \text{ k}\Omega$.

TABLE II NOISE FIGURE FROM FIG. 10 at $R_{src,p} = 100 \ k\Omega$

$L_{src,p}$	Von	W_{eff}	NF
[nH]	[mV]	[µm]	[dB]
	100	1240	1.06
	150	1240	0.88
500	200	1240	0.80
	250	1240	0.77
	100	880	0.67
	150	880	0.52
700	200	880	0.45
	250	880	0.42
	100	720	0.53
	150	720	0.39
900	200	720	0.32
	250	720	0.28

performance is achieved. This latter point means that we can consume less power (because for a given V_{on} , a device with smaller W_{eff} draws less current) for a given noise figure with a larger effective (parallel equivalent) source inductance $L_{src,p}$.

This is rather good. In a previous technical note [1] we found that our matching network should convert our source to $R_{src,p} = 0.37 \text{ M}\Omega$ and $L_{src,p} = 871 \text{ nH}$ for optimum gain.

So, finally, we ask what if our matching network converted our given source ($R_{src} = 1.7 \ \Omega$, $L_{src} = 56 \ nH$) into a source with $R_{src,p} = 100 \ k\Omega$ and $L_{src,p}$ set such that it resonates out the capacitive reactance seen looking into the LNA (at 200-MHz). The results are shown in Fig. 11 where the black line denotes V_{on} and W_{eff} combinations at which a noise figure of 0.5 dB is realized.

The results are very encouraging, with a very broad design space capable of giving us noise figures of less than 0.5 dB. And because we are working with an $R_{scr,p}$ of 100 k Ω and imaginary impedance components that resonate out (at 200-MHz) we can expect a gain degradation of only about 6 dB.

The gain results are shown in Fig. 12 where the black line denotes a 30-dB gain and the red line denotes the gains at



Fig. 11. The NF for a CS LNA driven by a source whose parallel equivalent resistance is $R_{src,p} = 100 \text{ k}\Omega$ and whose parallel equivalent inductance, $L_{src,p}$ is set to resonate out with the capacitive input impedance of the amplifier.



Fig. 12. The gain for a CS LNA driven by a source with series equivalent $R_{src} = 1.7 \ \Omega$, $L_{src} = 56 \ \text{nH}$ which is transformed into a source with $R_{src,p} = 100 \ \text{k}\Omega$ and an imaginary component which resonates out with the imaginary component of the LNA input impedance at 200 MHz.

which a noise figure of 0.5 dB is realized. These are extremely encouraging results. The cross section of the red and blue lines occurs at approximately $V_{on} = 140$ mV and $W_{eff} = 800 \ \mu\text{m}$ at this point out gain is 30 dB and NF is 0.5 dB, but we can do much better. For instance, at $V_{on} = 200$ mV and $W_{eff} =$ $560 \ \mu\text{m}$ we maintain our 30-dB gain, but drop the noise figure to 0.26 dB. There is a fair amount of room for optimization here.

For the record, the matching network used to realize this is the same one discussed in [1]. It is shown again in Fig. 13 for convenience. As discussed before [1] the component values for this matching network are not unreasonable although the inductor will have to be implemented off-chip.

The thoughtful student should approximate the losses to be



Fig. 13. Gain matching network B (GMB).

encountered in such a matching network and double check all the results presented in this technical note.

REFERENCES

- [1] S. Magierowski, "Common-source LNA: Gain," Tech. Rep., July 5 2007.
- [2] D. G.-W. Yee, A Design Methodology for Highly-Integrated Low-Power Receivers for Wireless Communications, Ph.D. dissertation, University of California, Berkeley, Spring 2001.
- [3] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, Cambridge, 2nd edition, 2004.
- [4] A. A. Abidi, "High frequency noise measurements on FET's with small dimensions," *IEEE Trans. Electron Devices*, vol. 43, no. 11, pp. 1801– 1805, Nov. 1986.
- [5] A. J. Scholten, L. F. Tiemeijer, R. van Langevelde, R. J. Havens, A. T. A. Zegers van Duijnhoven, and V. C. Venezia, "Noise modeling for rf cmos circuit simulation," *IEEE Trans. Electron Devices*, vol. 50, no. 3, pp. 618–632, Mar. 2003.
- [6] L. Belostotski, "Personal communication," June 2007.