Fabricating Integrated Monopoles

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***Abstract*— A brief discussion on the possible construction of integrated monopole antennas for mm-wave applications.**

I. Introduction

The dipole antenna is a classic radiative structure. The advantage of this (at least the monopole version) compared to planar antennas is that it should be possible to very effectively shield the monopole from the losses of a silicon IC substrate. The problem, of course, lies with the construction of substantial vertical structures on an integrated platform. This problem has been so significant as to preclude any significant work on integrated monopoles in the past.

II. Monopole Calculations

Before considering the actual fabrication of dipole antennas on a chip, we pause to approximate the rough monopole characteristics needed to support mm-wave signalling.

A. Radiation Resistance

First, the free-space wavelength of signals between 30 GHz and 60 GHz ranges from 10 mm to 5 mm. For a quarter-wave monopole over a ground plane we are then considering heights of only 2500-μm to 1250-μm. Using the rough estimate presented in [1]

$$R_r \approx 40\pi^2 \left(\frac{l}{\lambda}\right)^2 \tag{1}$$

where l is the length of the monopole, we can expect radiation resistances around 25 Ω for quarter-wave monopoles.

B. Ground Plane

If we target a 0.18-μm CMOS technology the ground plane for the monopole will most likely be constructed using metal6 (M6) a 2.34-μm thick aluminum conductor with a sheet resistance, R_{sh} of 0.0178 Ω/sq (nominal) hence a conductivity of

$$\sigma = \frac{R_{sh}}{t} \tag{2}$$

where t refers to the metal thickness. Thus, M6 has a conductivity of 2.4×10^7 $\mho$/m.

We expect that a suitable ground plane needs to have a radius of about $\lambda/4$. Since the wavelength with respect to the ground plane is dependent on the substrate, we must consider the materials on which the ground plane is deposited.

M6 rests on 8.15-μm of dielectric material (nominal) with an average relative dielectric constant of $\epsilon_r = 3.81$ (and a conductivity of approximately 10^{-5} $\mho$/m). Below this lies about 730-μm of silicon substrate with a resistivity of 10-Ω·cm (corresponding to a p-type doping concentration of $1.7 \times 10^{15}\text{cm}^{-3}$), hence a conductivity of about 10-$\mho$/m. The relative dielectric constant of the silicon is 11.7.

Many thanks to the friends of FishLab.

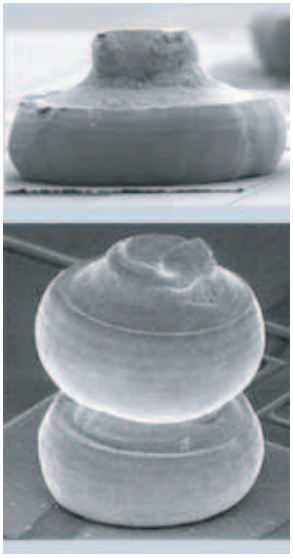

Fig. 1. An SEM photograph of a single bump and a stack of two bumps.

Approximating the composite dielectric constant of the oxide-silicon substrate as simply 11.7 and using

$$\lambda = \frac{1}{f\sqrt{\epsilon_r \epsilon_0 \mu_0}} \tag{3}$$

where $\epsilon_0 = 8.854 \times 10^{-12}$ F/m and $\mu_0 = 4\pi \times 10^{-7}$ H/m we find that the quarter-wave extent of the ground plane is 730 μm for 30-GHz signals and 365 μm for 60-GHz signals. With strategic active circuit placement either option can be affordably accommodated on-chip.

III. Fabrication

The monopole fabrication technique to be explored is conceptually simple: a stack of solder bumps, one atop the other. Fig. 1 provides an idea of one bump as well as a two bump stack. In Fig. 2 we see an example of seven bumps stuck (about 240-μm high) one atop the other. According to Bob Stevenson of the CMC, the current vendors with whom CMC is dealing with can reliably (no definite measure to this statement is available) stack 7-8 stud bumps and had stacked as many as 15 (within an expected drop in repeatibility).

A stud bump normally bulges out 70-μm in diameter. To accommodate for the bonding tool footprint, Mr. Stevenson suggests that the minimum pitch for the pads be 125 μm in one dimension and 200 μm in the other. The pad size for a bump should be at least 75 μm square. Each solder bump

Fig. 2. A stack of seven bump studs.

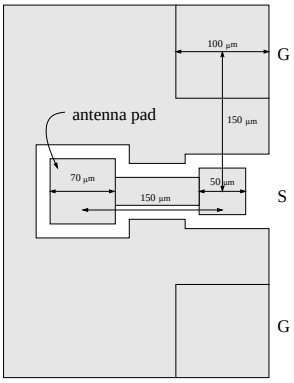

Fig. 3. A single monopole layout.

is about 30 to 35 μm. The bumps are made out of 24 karat gold (conductivity around 4.55×10^7 $\mho$/m) and are sometimes alloyed with 0.1% silicon.

IV. Proposed Teststructures

A large variety of tests can be performed to study the properties of the antennas under consideration. A simple and straightforward connection consists of a dipole antenna driven by a GSG on-wafer probe for the purpose of S_{11} characterization. A possible layout of this set-up is illustrated in Fig. 3.

In this design a short on-chip coplanar waveguide connects the GSG probe to the antenna. Potential issues with radiation from the GSG probe have to be considered, although it is assumed that a careful calibration can factor out this affect.

An alternative monopole test structure can have the antenna entirely surrounded by an M6 ground plane, with a signal fed in from any bottom metal. This feed structure can be surrounded by ground-planes both above and below.

References

[1] T. H. Lee, *Planar Microwave Engineering*, Cambridge, 1st edition, 2004.