The Noise of a CMOS Reflector: Long-Channel Approximation

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***Abstract*—The noise of a CMOS reflector using a simple long-channel MOSFET approximation.**

I. Introduction

One technical note [1] discussed the gain and phase characteristics of a reflection node (for phase-transmit diversity) from a high level. A follow-up technical note [2] proposed a simple MOSFET circuit for the reflector. A sketch of this circuit is shown in Fig. 1. The parallel RLC circuit is the sum total of the antenna and extraneous circuitry needed to affect phase modulation. The resistance R_p is the parallel equivalent resistance of the antenna including both radiative and ohmic losses. The relation between R_p and the antenna conductance is simply $G_A = 1/R_p$.

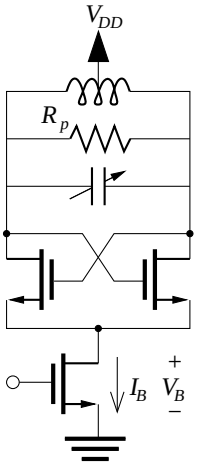

Fig. 1. The MOS reflector node.

II. The Reflector Circuit

A third technical note [3] helped outline some of the design space for the reflector in a phase-sweep transmit-diversity scheme discussed in [4]. That work considered the system operating at 5.5 GHz on a small loop antenna with $R_p = 13.9$ kΩ, an inductance of 11.2-nH and capacitance of 80.7-fF [5]. Assuming a simple power supply of $V_{DD} = 1$ V and a bias transistor voltage drop of $V_B = 200$ mV, the net dc power needed to affect a compensation factor of $K_G = 0.95$ (for the antenna under consideration) requires a $P_{dc} = 35.4$ μW.

Many thanks to the friends of FishLab.

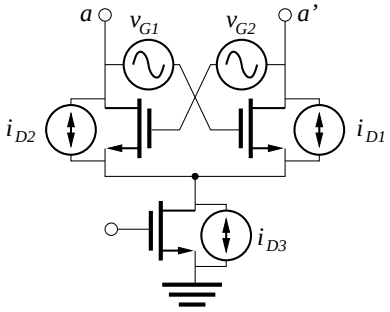

Fig. 2. The MOS reflection amplifier with internal noise sources.

This setting prompts a bias current of $I_B = 35.4$ μA and a MOSFET transconductance (for the cross-coupled pair) [2]

$$g_m = \frac{I_B}{V_{on}} = \frac{I_B}{V_{DD} - V_T - V_B} \tag{1}$$

where V_T is the threshold voltage of the amplifying transistors and is taken to be approximately 0.5 V. These settings result in $g_m = 70.8$ μS, a value useful to a more in-depth circuit analysis.

A. Noise Factor Expression

An earlier technical note [6] derived the noise factor for a general one-port reflection amplifier

$$F = 1 + \left(1 - \frac{1}{|S_{11}|^2}\right)\frac{-P_e}{kTB}. \tag{2}$$

where $-P_e$ (a positive value) is the amplifier's available noise power and

$$S_{11} = G = \Gamma_c = \frac{(1+K_G) - j(1+K_B)Q_A}{(1-K_G) + j(1+K_B)Q_A}. \tag{3}$$

in which $Q_A = B_A/G_A$, $K_G = -G_C/G_A$, $K_B = B_C/B_A$ ($Y_C = G_C + jB_C$ is the admittance of the circuit attached to the antenna and $Y_A = G_A + jB_A$ is the admittance of the antenna itself).

B. Circuit Noise Components

In order to calculate $-P_e$ we have to identify the noise sources in more detail. To see this we refer to Fig. 2 where the amplifier circuit alone is shown along with the drain current and gate voltage noise sources.

All the noise sources are assumed to be white gaussian random variables. The spectral density of the MOSFET current noise (i.e. referring to i_{D1}, i_{D2}, i_{D3} is given by [7]

$$\frac{\overline{i_D^2}}{\Delta f} = 4kT\gamma g_{d0} \tag{4}$$

where k is Boltzmann's constant, T is the temperature, and g_{d0} is the MOSFET's channel conductance for V_{DS} = 0. The factor, γ, is a measure of the conductive channel's shape. For long channel devices, $\gamma = 2/3$, in a nod to the presence of other noise sources (e.g. source/drain-region thermal noise) we will take $\gamma = 1$.

For devices biased in saturation (the case for our circuit) we can re-write the current-noise expression as

$$\frac{\overline{i_D^2}}{\Delta f} = 4kT\gamma g_m \tag{5}$$

which, at 290 K for the circuit under consideration (g_m = 70.8 μS for the cross-coupled MOSFETs) gives $\overline{i_D^2}/\Delta f = 1.13 \times 10^{-24}$ A^2/Hz for the reflecting transistors. The noise of the tail bias transistor need not concern us since it is only a common-mode disturbance (and therefore not coupled to the differential signals).

The voltage noise density at the gates of the cross-coupled transistors consist of at least two components, the drain-induced gate noise and the gate resistance noise. In this analysis we will only consider the latter which is simply [7]

$$\frac{\overline{v_G^2}}{\Delta f} = 4kTR_G \tag{6}$$

where

$$R_G = \frac{1}{3}\frac{1}{4}\frac{W_{ch}}{L_{ch}}\frac{R_{sh}}{n} \tag{7}$$

where R_{sh} is the sheet resistance of the gate material (silicided polysilicon, about 5 Ω/sq), n is the number of gate fingers and W_{ch} and L_{ch} are the channel gate width and length, respectively. The factors 1/3 and 1/4 account for the effects of distributed resistance and the effect of shorting the gate strips on both sides of the MOSFET, respectively.

Assuming $L_{ch} = 0.2$ μm we can calculate W_{ch} according to

$$W_{ch} = \frac{g_m L_{ch}}{\mu_n C_{ox} V_{on}} \tag{8}$$

where the mobility μ_n is approximately 150 cm^2/V·s and $C_{ox} \approx 0.72$ μF/cm^2 (for a 0.18-μm CMOS technology). Using the values for g_m (70.8 μS), V_{on} (0.5 V), and L_{ch} (0.2 μm) given above we find W_{ch} = 0.26 μm. This is clearly impractical (for one the foundry does not even provide models for devices with such width, values $\gtrsim 1$ μm are more common), but gives us a sense of the ratio W_{ch}/L_{ch} needed to ultimately calculated the gate voltage noise. This then comes to $\overline{v_G^2}/\Delta f = 8.67 \times 10^{-21}$ V^2/Hz for $n = 1$.

C. Differential Reflector Noise

Having identified and quantified the individual noise components in the circuit, we have yet to lump them into a single differential noise source from which we can obtain a circuit-based expression for $-P_e$ and from which we may finally calculate the noise factor through Eq. (2).

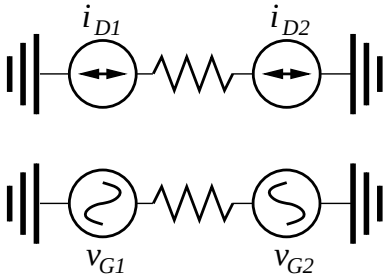

Fig. 3. Simplified equivalent of circuit noise sources interfaced to antenna loss (remainder of antenna and circuit omitted).

The situation we are faced with is essentially the one sketched in Fig. 3. That, is our load (represented only with the net antenna resistance R_p for simplicity) is driven to either side by uncorrelated white noise sources. In transforming the given sources to differential equivalents we will rely on rough heuristic arguments rather than a rigorous development.

Invoking the superposition principle we begin by considering the current sources alone. Here we can imagine that the total current through the resistance is the average of the two currents, that is

$$i_D = \frac{\pm i_{D1} \pm i_{D2}}{2}. \tag{9}$$

Since the two current source random variables are uncorrelated a mean-square operation gives

$$\frac{\overline{i_D^2}}{\Delta f} = \frac{\overline{i_{D1}^2}/\Delta f + \overline{i_{D2}^2}/\Delta f}{4} = 2kT\gamma g_m. \tag{10}$$

Thus, the net differential noise contribution due to the MOSFET drain current noise for the specific reflector design under consideration is 5.65×10^{-25} A^2/Hz.

The gate voltage sources can be treated in a similar manner, that is

$$\frac{\overline{v_G^2}}{\Delta f} = \frac{\overline{v_{G1}^2}/\Delta f + \overline{v_{G2}^2}/\Delta f}{4} = 2kTR_g. \tag{11}$$

To place both sources on the same footing we convert the equivalent differential gate voltage source, into a current source via

$$\frac{\overline{i_G^2}}{\Delta f} = \frac{\overline{v_G^2}}{\Delta f R_p^2} = \frac{2kTR_g}{R_p^2}. \tag{12}$$

Using the values given above we thus calculate $\overline{i_G^2}/\Delta f = 2.24 \times 10^{-29}$ A^2/Hz. Obviously, the gate noise is negligible compared to the drain noise in this design. We will ignore it for the remainder of this technical note.

III. Reflector Noise Calculations

The maximum exchangeable noise power from the reflection amplifier is

$$-P_e = \frac{\overline{i_D^2}}{\Delta f}\frac{R_p K_G}{4} B. \tag{13}$$

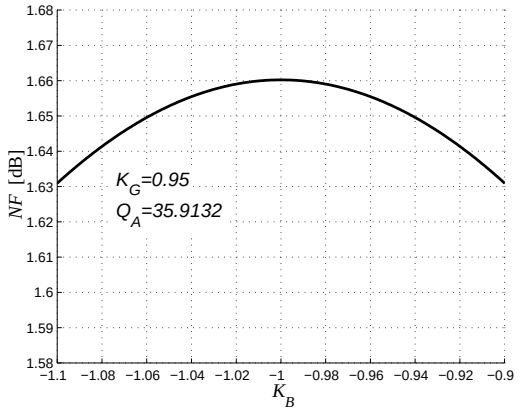

Fig. 4. The noise figure of a cross-coupled reflection amplifier built out of 0.18-μm CMOS technology and driving a 6-mm loop antenna.

With this and Eq. (2) we are at last able to to calculate the noise figure for the reflection amplifier under consideration. The results are shown (as the noise figure $NF = 10\log(F)$) in Fig. 4.

As compared to CMOS LNAs consuming ~ 10 W the 1.6-dB noise figure of the reflection amplifier (which consumes only 35.4 μW) is excellent. What influence this has exactly on the PSTD scheme has yet to be determined.

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