EECS2210: Electronic Circuits & Devices

Lab #5

A Common Source MOSFET Amplifier

Introduction and Objective

The objective of this experiment is to explore two stage MOSFET amplifiers.

Goals:

1. Analyze and test a MOSFET based amplifier.

2. Discuss common MOSFET applications.

Hand Calculation and Prelab

1. Consider the circuit shown in Fig. 1.

   a) Assume both transistors are in saturation. Find I_{D1}'s expression in terms of V_{DD} and R_B, μ_n, C_{ox}, V_{TH1}, and W_1/L_1.

   b) As shown in the circuit, M1's Gate is connected to M2's Gate, and the Source terminal of the two devices are also connected to the same terminal (i.e., ground). If the two transistors have the same μ_n, C_{ox}, V_{TH}, and W/L, what is the relationship between I_{D1} and I_{D2}?

   c) What will be the relationship if W2/L2 = 5 * W1/L1?

   d) Try to draw a circuit with similar functionality but using two PMOS transistors instead of two NMOS transistors.

   e) Assuming $\mu_n C_{ox}$ = 0.5mA/V^2, VDD=5V, V_{TH}=0.4V, W1/L1=5, and W2/L2 = 25, find R_B that results in I_{D2} = 10mA.

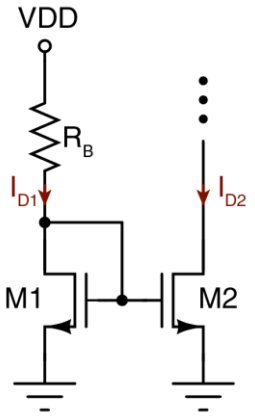

Fig.1. Circuit schematic of a current mirror implemented using two NMOS transistors.

2. Consider the circuit shown in Fig. 2. Draw the small-signal equivalent circuit and find the small-signal gain expression.

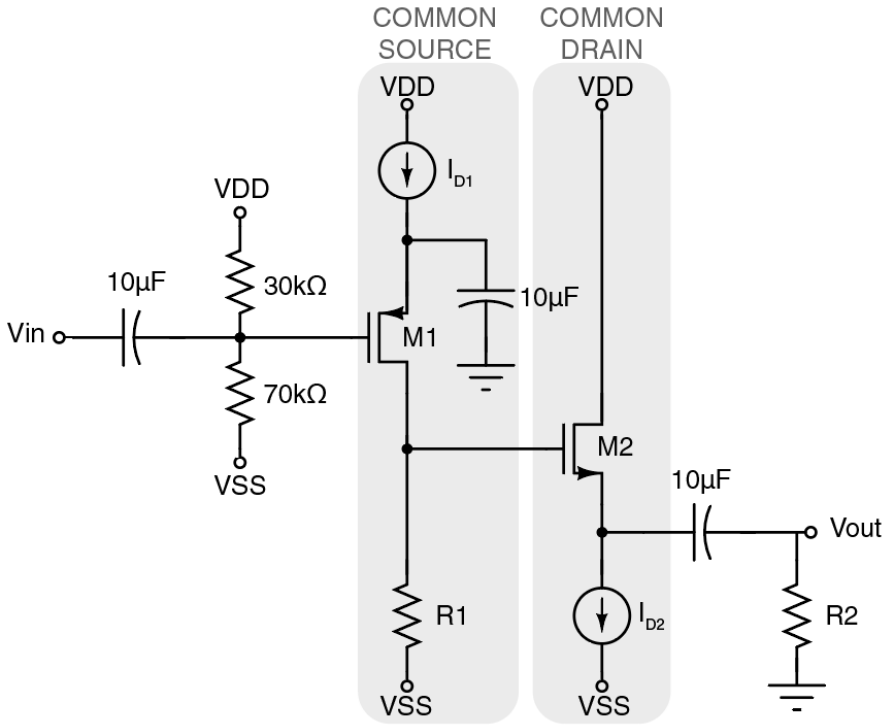

Fig. 2. Two-stage CS + CD amplifier.

Background

The objective of this experiment is to perform a basic transistor-level design of a multistage amplifier. A general amplifier is shown in Fig. 3(a) and the equivalent circuit is shown in Fig. 3(b). The signal source is set to provide a sinusoidal waveform with a peak-to-peak voltage of approximately 100 mVp-p. This is a typical output from many types of sensors that require amplifiers including Microphones, Accelerometers, and Thermocouples. As discussed in lectures, an amplifier must meet the following specifications simultaneously:

- High gain
- High input resistance
- Low output resistance

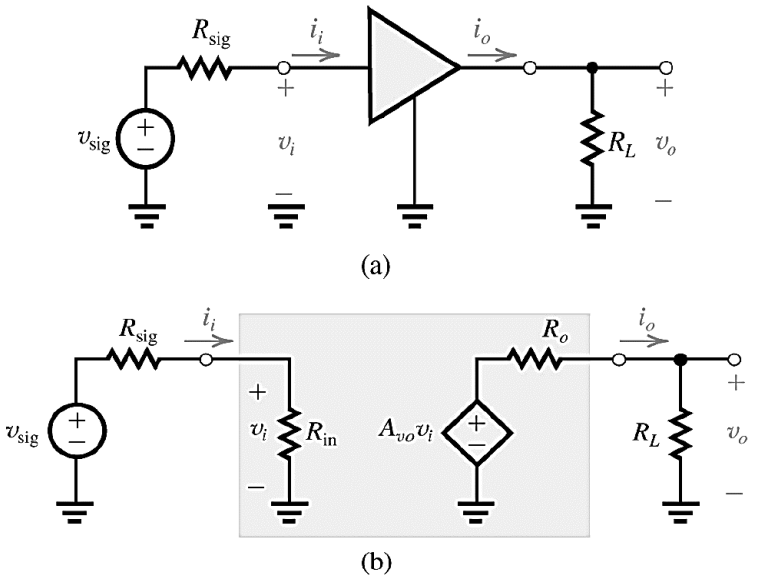

Fig. 3. (a) Functional block of an amplifier and (b) equivalent circuit representation.

Achieving these three characteristics with a single-stage MOSFET amplifier is not practical. Instead, we employ the cascaded amplifier approach, where the first stage has high input resistance and high gain, while the second stage provides low output resistance to drive the load resistance. The three most common MOS amplifier configurations are shown in Fig. 4.

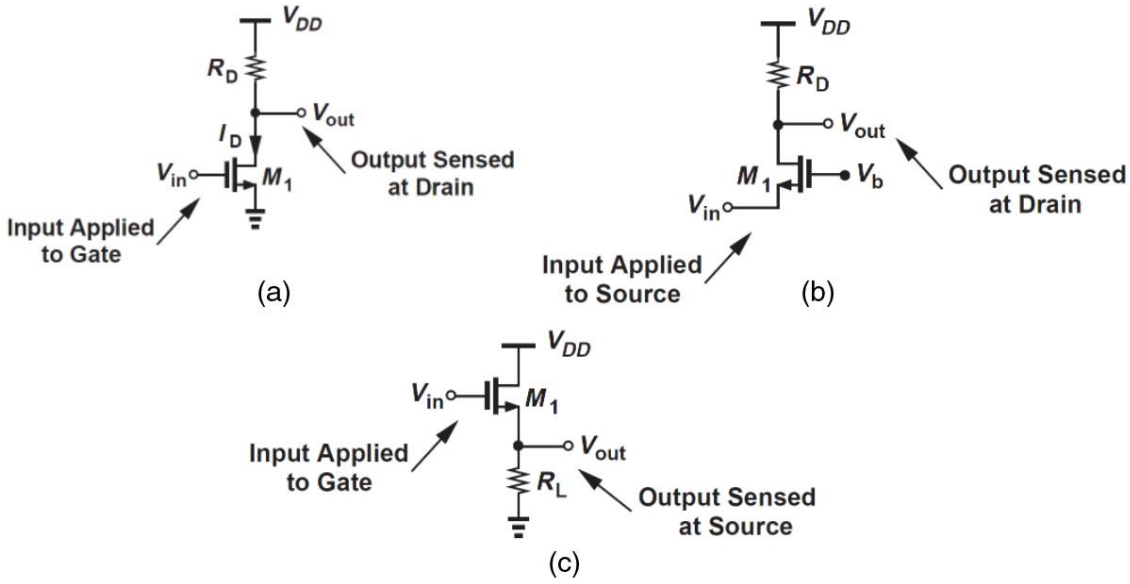

Fig. 4. Three basic MOSFET amplifier configurations: (a) common source, (b) common gate, and (c) common drain.

Based on the characteristics that we learned about these amplification stages, in this lab, we will use a common-source amplifier for the first stage to get high input resistance and high gain, and a common drain amplifier for the second stage to get the low output resistance. The cascade of the two stages will result in a two-stage amplifier as shown in Fig. 5, where A_1 and A_2 are the voltage gain of the first and second stages, respectively. A transistor-level implementation of this circuit is shown in Fig. 2.

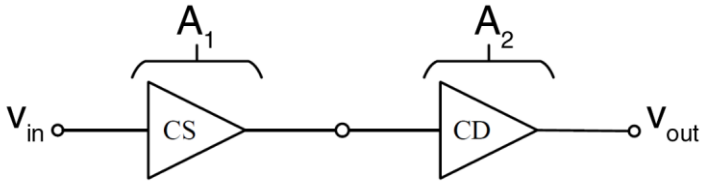

Fig. 5. Functional block diagram of a two-stage MOSFET amplifier.

The full schematic for the configurable two-stage amplifier is shown in Fig. 6. This is the same circuit as what was shown in Fig. 2, except that the ideal current sources are replaced with real circuits made from transistors. These circuits are designed based on the current mirror we studied in Fig. 1, as described below.

As shown, M3 is diode connected (that is, its drain and gate are connected). If we write a KVL from VDD through R_{B1} and M3 to VSS, we will find that the drain current of M3 as:

$$I_{D3} = \frac{VDD - VSS - V_{GS3}}{R_B} \quad (1)$$

This means that I_{D3} can be easily adjusted by varying the value of R_B, thus it make sense to use a potentiometer (i.e., a variable resistor) for R_B, as shown in Fig 6. Also shown in Fig. 6, Gate of M3 is connected to the Gate of M4, M5, M8, and M9, making them current mirrors (see Fig. 1). This means that if these transistors are identical to M3, their drain currents will also be identical to M3's. The switches S1 and S2 allow us to set the I_X to I_{D3} (if only one switch is closed) or $2\times I_{D3}$ (if both switches are closed). Note that I_X is equal to I_{D6}, and since M6 and M7 have a current mirror configuration, $I_{D7}=I_{D6}=I_X$. The above discussion shows that we can replace the ideal current source (I_{D1} in Fig. 2) with a transistor-based circuit, and the current can be adjusted using equation (1) and switches S1 and S2.

Similarly, I_{D2} is replaced by a transistor-based circuit that generates either I_{D3} or $2\times I_{D3}$ depending on which one of S3 and S4 are connected.

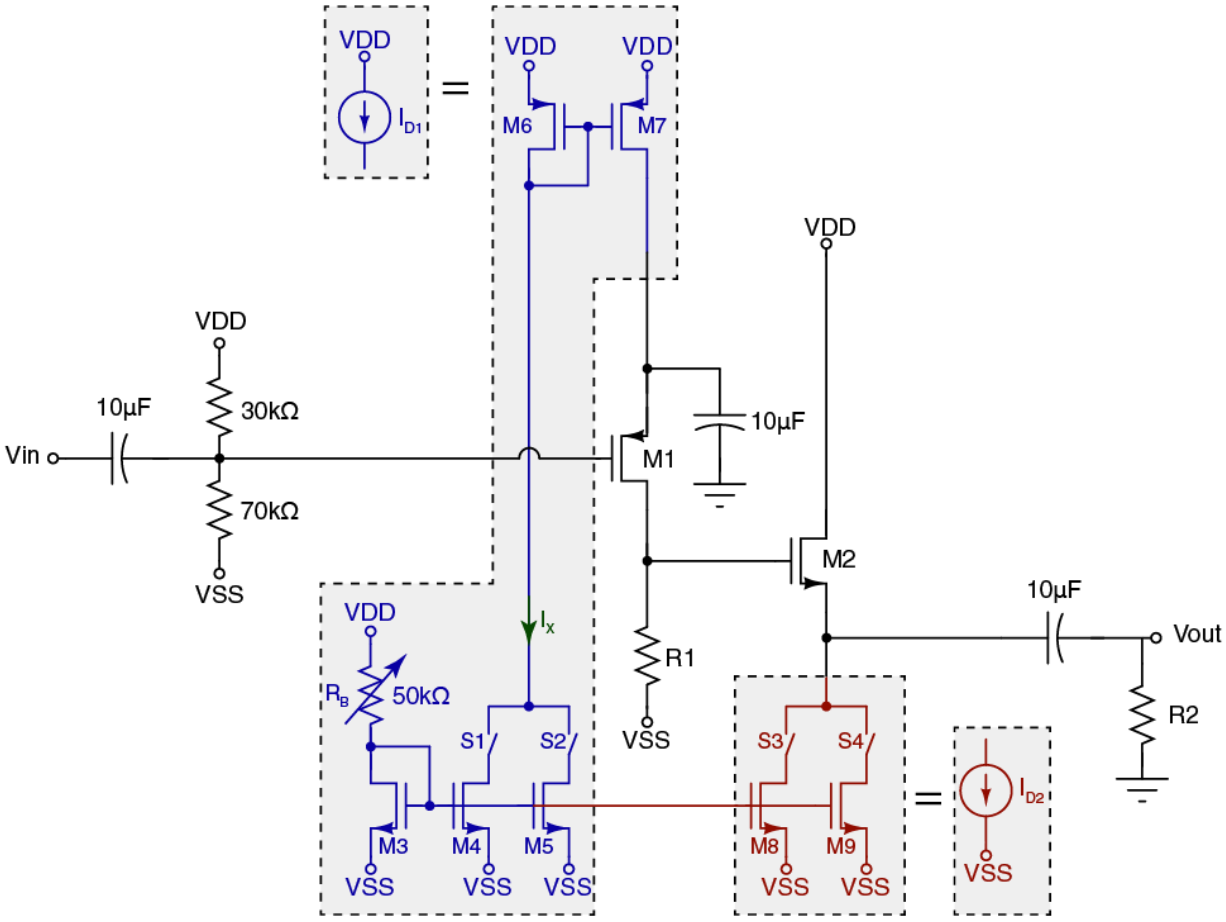

Figure 6. Full schematic of the two-stage amplifier.

Lab Experiments

In this portion of the lab we will use the circuit shown in Fig. 7 to investigate the behavior of a two-stage CMOS amplifier.

1. Build the circuit as shown in Fig. 7 phase by phase. Set all the variable resistors to 0 ohm. Set Vdd = 5V, VSS = -5V. Connect the substrates of the PMOS devices to Vdd and NMOS devices to VSS. Using a multimeter, measure the DC voltage at V1, V2, and V3. Based on your measurements, what is the operating mode for transistors M1 and M2. Note that you need to calculate the gate voltage of M1 based on the resistive voltage divider shown in Fig. 7. You should build the circuit phase by phase as shown in Fig. 7. Measure the DC operating point in each phase. Ask your TA to check after you've done each phase.
2. Set the function generator to output a 0.1 Vp-p, 1 kHz, sine wave. This is a very small signal, so you will need to use the "SYNC" feature of your oscilloscope to lock the waveform. Do not connect to the circuit until you have checked right input is correct. Measure the small-signal gain of the first stage, Av1, and the second stage, Av2. Confirm that the first stage is inverting. Show your TA the input and output waveforms.
3. Gradually increase the gain of the first stage, Av1, by slowly increasing $R_{1\text{-}Var}$. Once you notice visible distortion at V2, stop increasing $R_{1\text{-}Var}$. Then try to adjust the bias current in M1 (use R_{B_var}) until the signal at V2 is no longer distorted. How does the drain current affect the gain based on your gain expressions from prelab calculations? Take note of which changes helped to decrease the output distortion. Now begin to slowly increase $R_{1\text{-}Var}$ again until you notice the distortion returning. Repeat the above process until you reach a gain of roughly 5 V/V without any output distortion. Write down the value of V2 used to achieve this gain. Show your TA the input and output waveforms.
4. Measure the second-stage gain, Av2. Vary R_{2_Var} and observe the effect on Av2. Does your observed effect of R_{2_Var} on Av2 match the prediction from your prelab calculations? Calculate gm2 (gm of M2) based on the observed gain. (Note that you may need to find the resistance of the potentiometer. To do this, turn off the power supply, and measure the resistance using the multimeter with the resistance setting.)

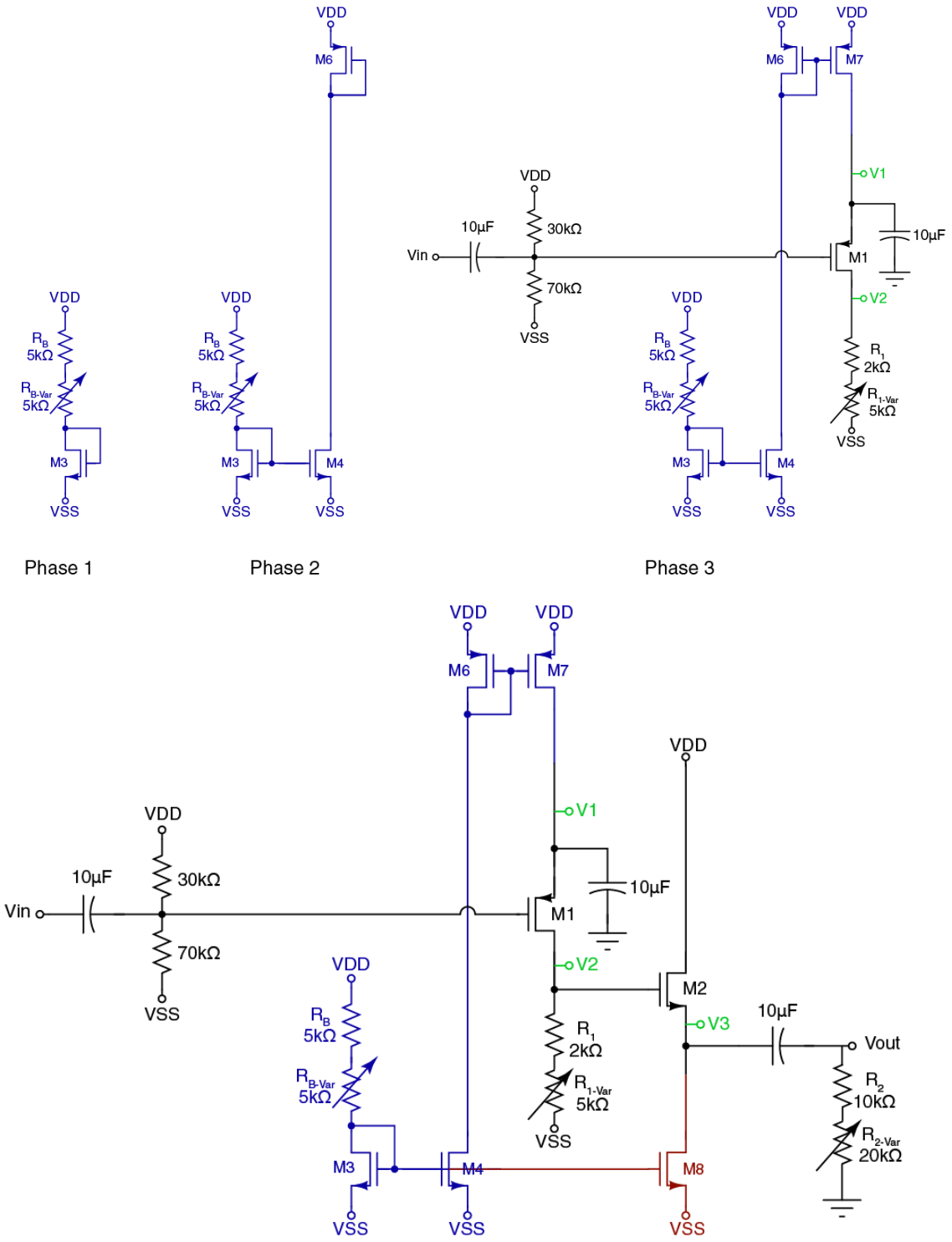

Fig. 7. Step by step construction of the two-stage amplifier.

Appendix

You will use ALD1101 and ALD1102 chips for NMOS and PMOS transistors, respectively. Each chip has two transistors. The chips' pin configuration is shown below.