# York University

## Department of Electrical Engineering and Computer Science

# Introduction to Simulation in Cadence

## EECS 4612

## Winter 2024-2025

## Introduction

This tutorial will guide you through the steps of creating a library, designing schematics, running simulations, and drawing layouts in Cadence. Follow the steps closely to familiarize yourself with the tool.

## Starting Up Cadence

**If you want to run cadence through your laptop or a EECS Windows PC:**

Go to Remote Lab (https://remotelab.eecs.yorku.ca/).

Use your EECS account to log in.

Select Remote Desktop (Crimson) or choose from one of the available "rl" hosts (rl01-rl25).

**If you want to run Cadence through an EECS Linux PC:**
You just need to login using your EECS account.

Once logged in, open a terminal and execute the following command create a folder in your home directory:

**********

mkdir ~/EECS4612

**********

*then change the created directory using this command:*

**********

cd EECS4612

**********

now to run cadence enter following command and press enter:

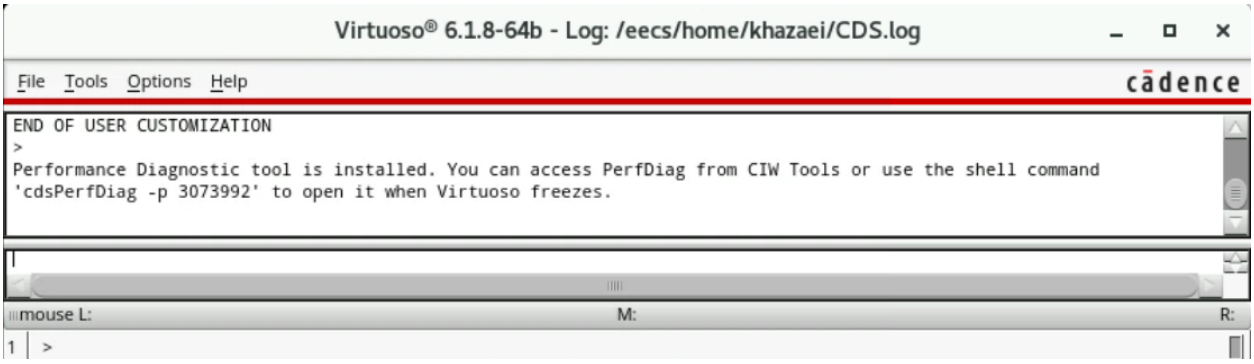
**********

gpdk45

**********

**Note:** It is always recommended to run Cadence inside the created directory

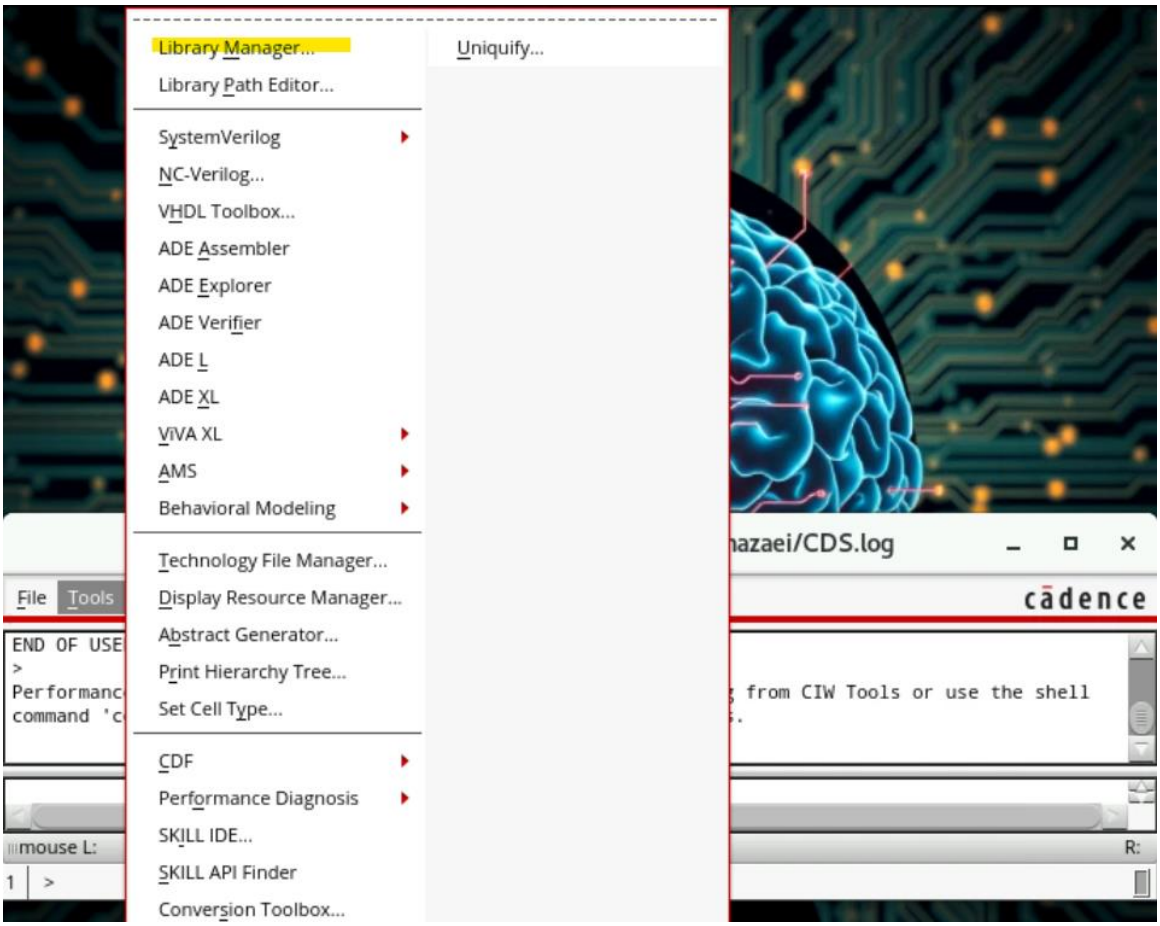
Wait for the software to open (CIW window).




## Creating a New Library in Cadence

### Open the Library Manager:

In the CIW window, go to the top menu and select Tools > Library Manager. This will launch the Library Manager window.



**Create a New Library:**

In the Library Manager, go to File > New > Library.

In the New Library window, enter the desired name for your library. For this tutorial, we will use "Test1".

Click OK to proceed.

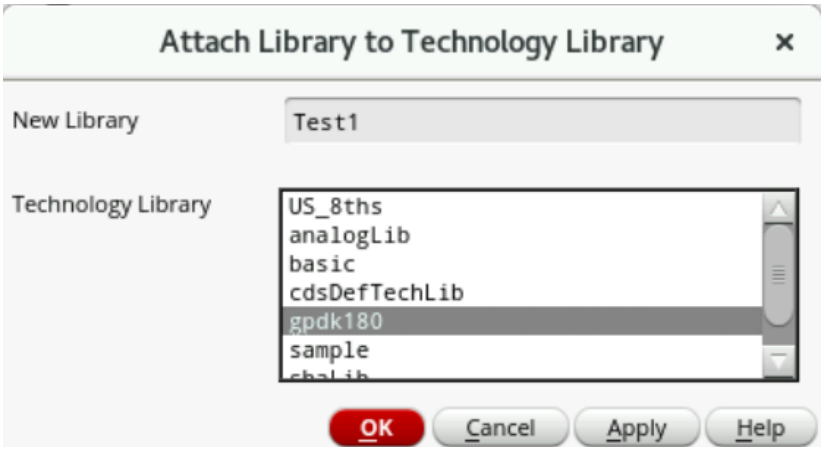
**Attach to an Existing Technology File:**

After clicking OK, a window labeled Technology File for New Library will appear.

Select Attach to an existing techfile and click OK.


**Select the Technology File:**

In the Attach Design Library to Technology File window, select the technology file (for example, gpdk180).



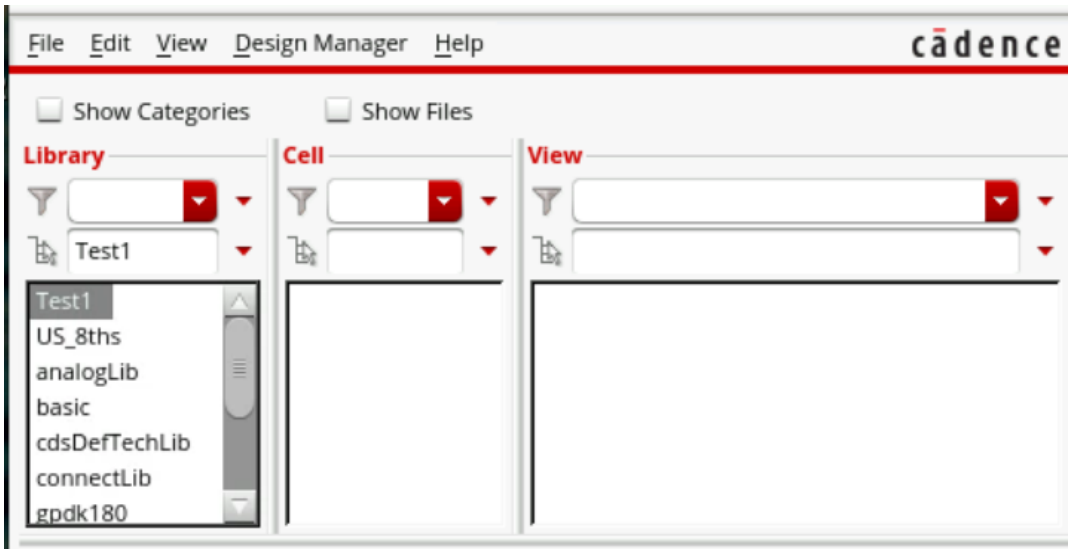

Click OK.

**Note:** In This tutorial gpdk180 is used. But in EECS4612 we work with 45nm technology- gpdk45. So, when you want to choose attached technology you have to select gpdk45. In future steps, whenever gpdk180 is mentioned, you must replace it with gpdk45.

**Confirm Library Creation:**

The new library should now appear in the Library Manager.

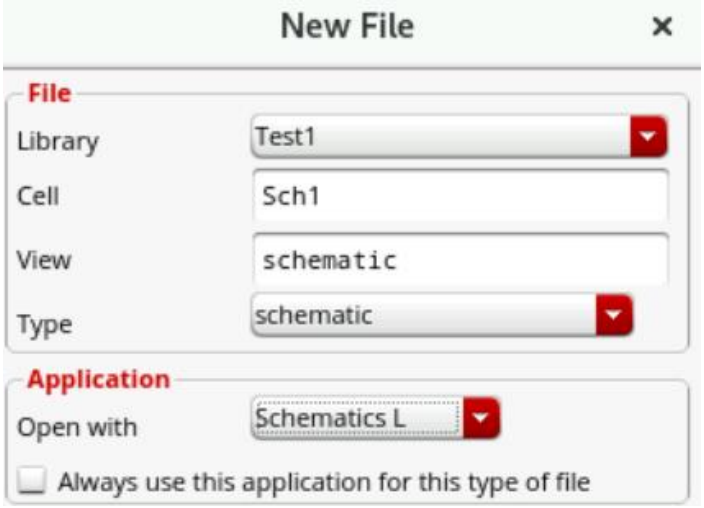
Your library is now ready to use with the attached technology file.



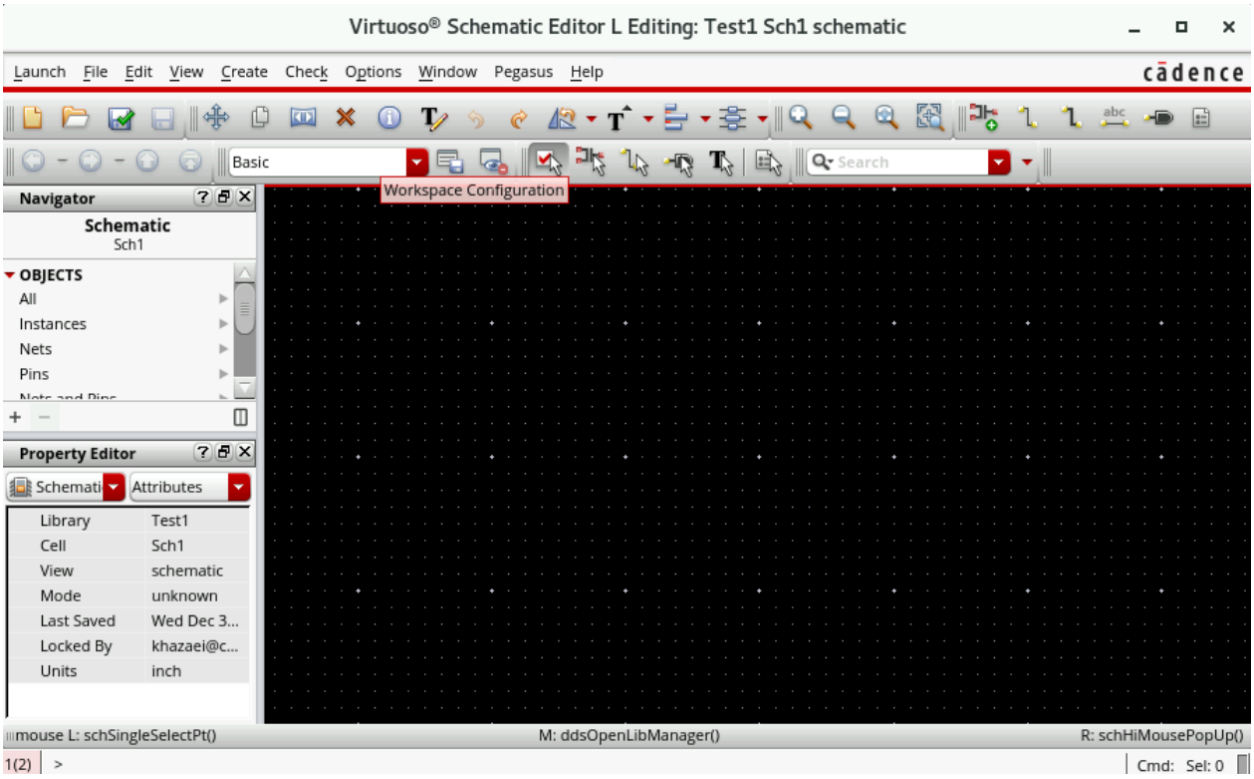

## Creating a Schematic

**Create a New Cell View:**

In the Library Manager, select your library (e.g., "Test1") and navigate to File > New > Cell View. In the Create New File window, enter a name for your design in the Cell Name field. We'll call it " Sch1".




Click OK to open the Virtuoso Schematic Editor.




**Design in the Schematic Editor:**

Familiarize yourself with the menu and hotkeys. For instance:

Press I to add components (instances).

Press W to draw wires.

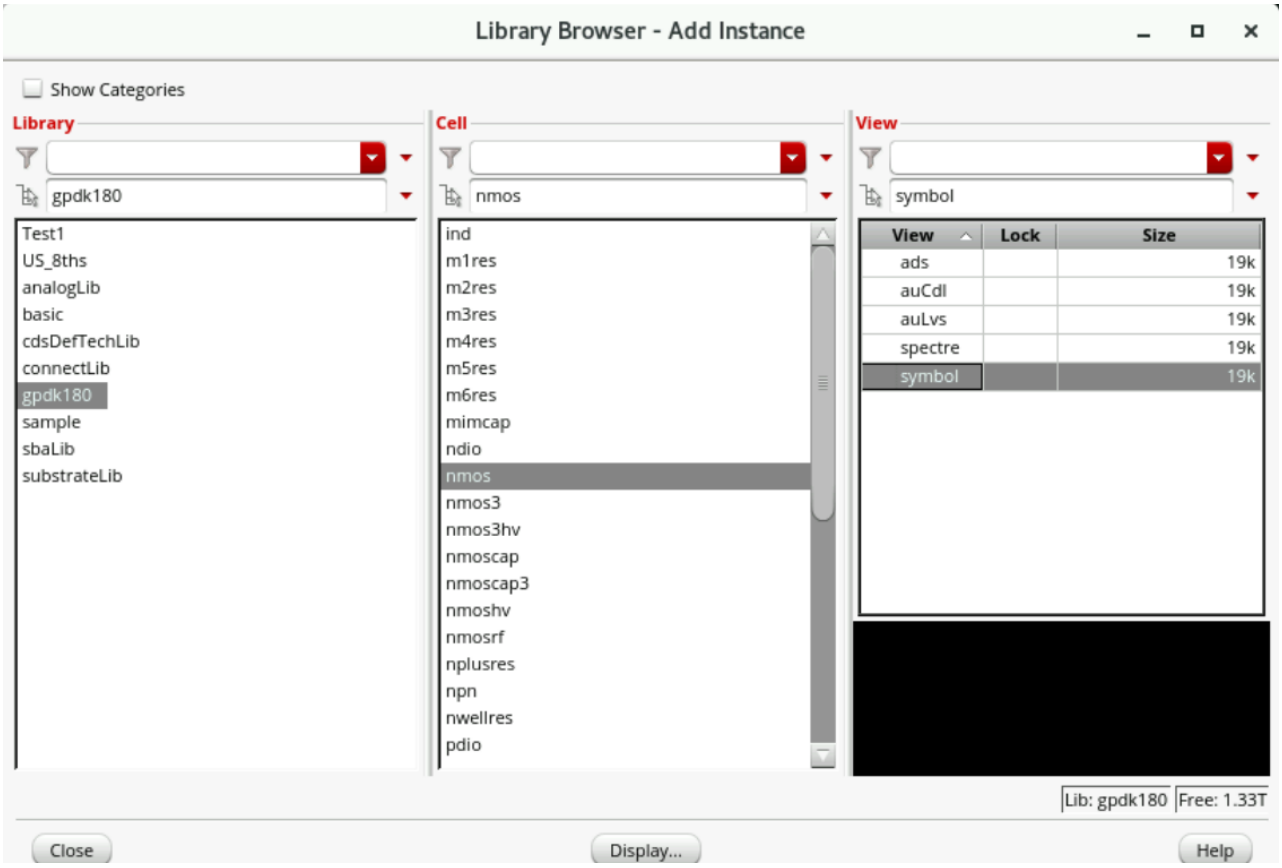
Press Q to modify properties of components.

## Add Components:

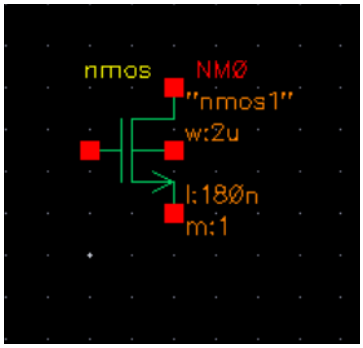
Press I to open the Add Instance window (or follow this: create > instance).

Select the library (gpdk180 for transistors), cell (e.g., nmos), and view (e.g., symbol).

Place the component in the schematic. For instance, place an NMOS transistor.



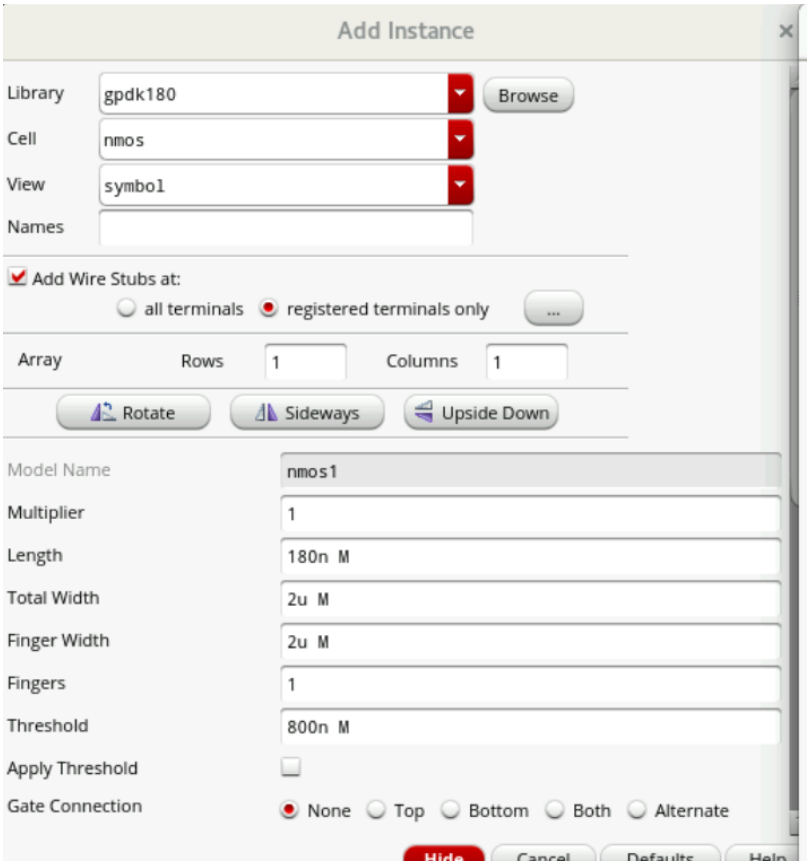

**Note:** In gpdk45 you will see different type of transistors. For your project you should use **nmos1v** and **pmos1v**.



Use **analogLib** library for components like voltage sources, ground, and others.

**Modify Component Properties:**

After placing a component, select it and press Q to modify its properties, such as W and L of transistors and DC voltages of a voltage source.



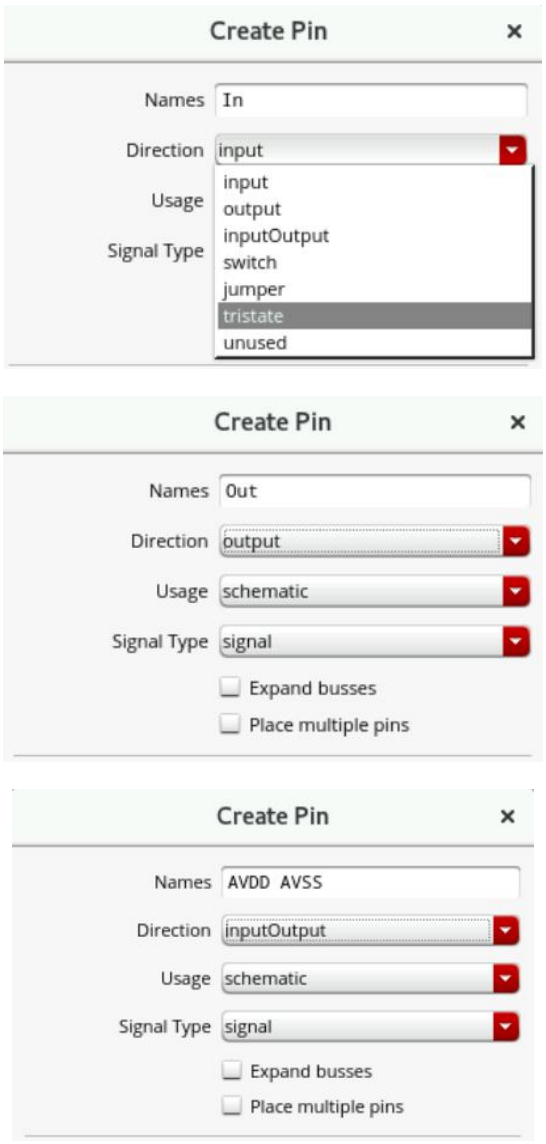

**Connect Components:**

Press W to wire your components. Click on a component terminal (indicated by red squares) and connect it to other components.

**Add Pins:**

Use Create > Pin to add pins for input, output, or supply.

Use input and output for regular connections and InputOutput for supply nodes like vdd and gnd!

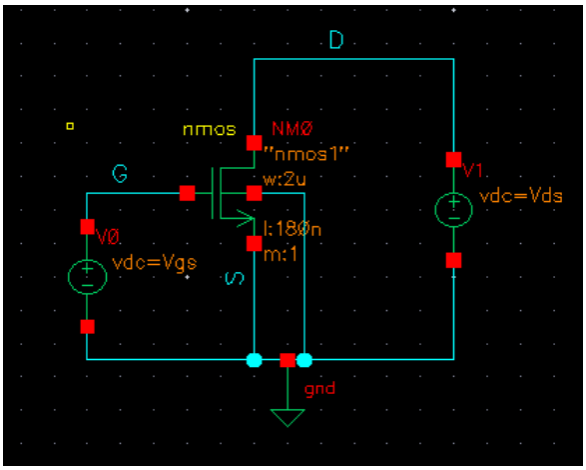



**Label Wires:**

Press L to label wires. Enter a name in the Names field and click on the wire you want to put label on it.

**Check and Save:**

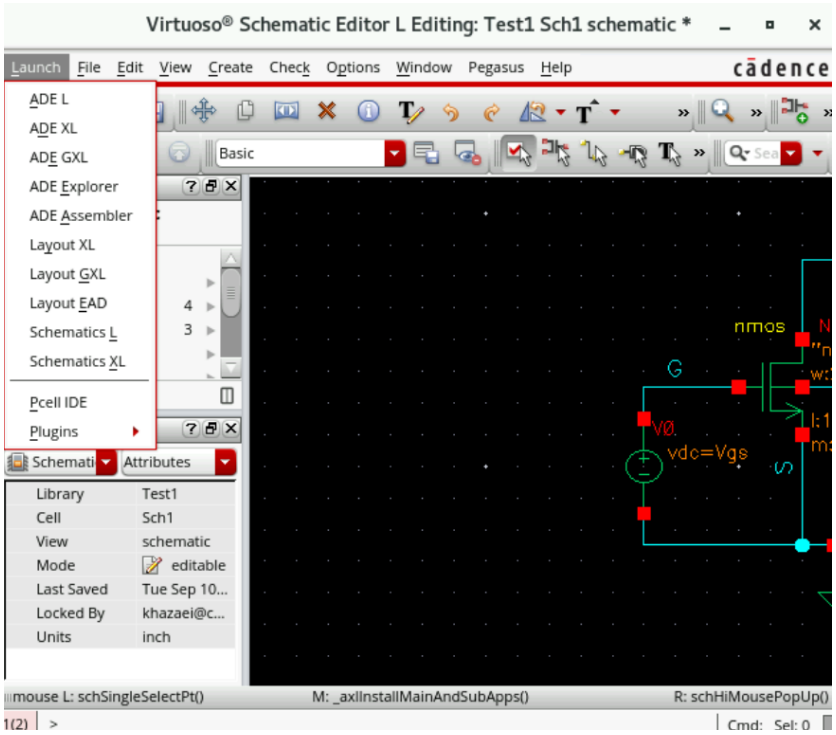
After designing your schematic, click the Check and Save button (a box with a check mark) to verify connections and save your work.




## Running a Simulation (DC, AC, Transient, …)

### Launch ADE (Analog Design Environment):

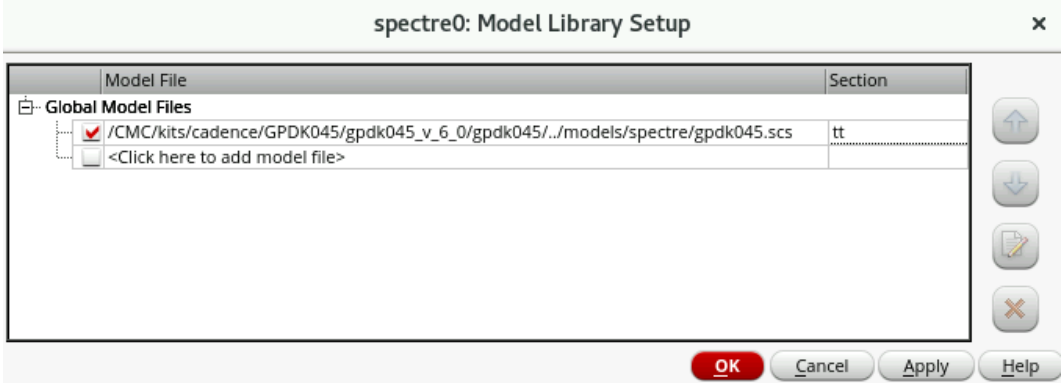
Open the simulation environment via Launch > ADE L




**Note:** If a popup window appears and asks you about the License just press **Always**.

**Set up transistor model libraries:**

Via Setup > Model Libraries and set the section to **tt**




**DC Analysis:**

Open the Choosing Analyses window via Analyses > Choose and select dc.

Check the Save DC Operating Point option and click OK.

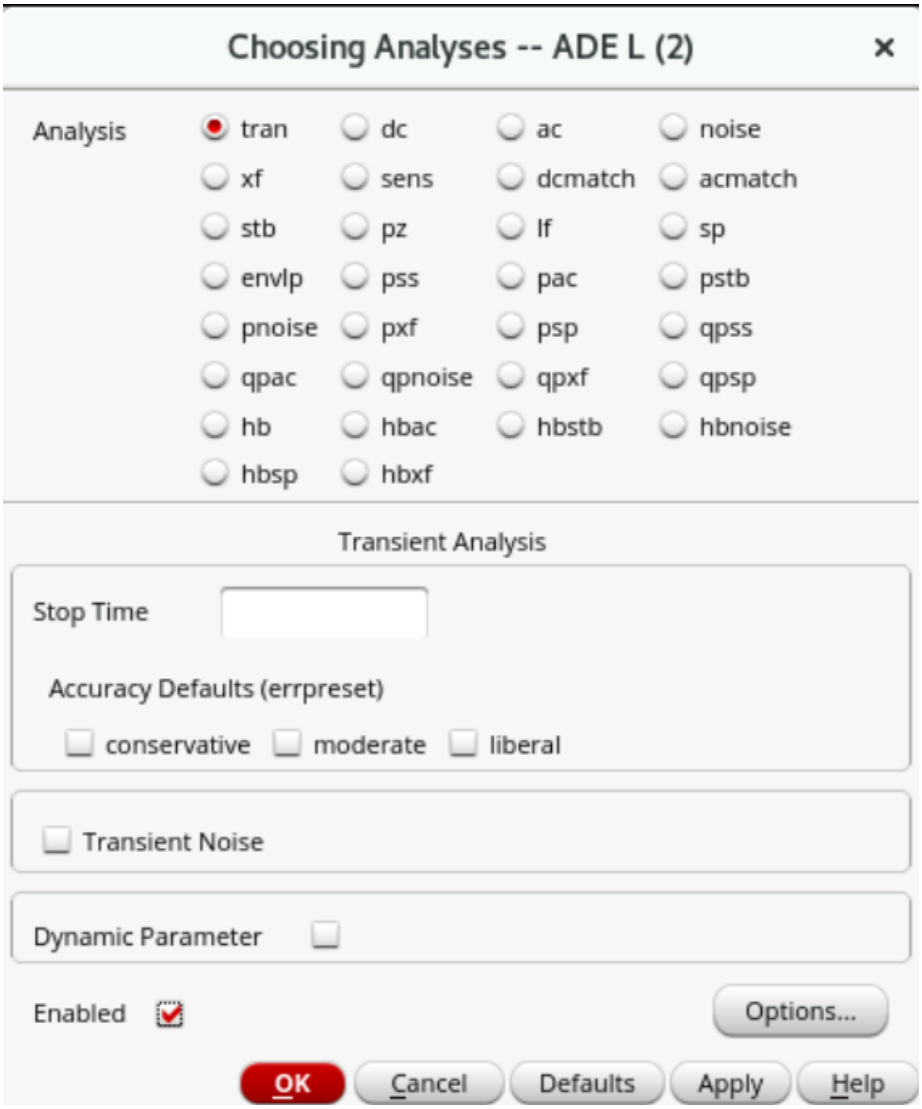
**AC Analysis:**

In the same Choosing Analyses window, select ac and configure the settings as needed.

**Transient Analysis:**

Select tran from the analysis options, set the stop time, and choose moderate accuracy.

Ensure Enable is checked.




**Run the Simulation:**

Click the Run button (green traffic light) to start the simulation.

**Viewing Results:**

Use the Results menu to view:

DC Voltages via Annotate > DC Node Voltages.

AC Voltage vs Frequency via Direct Plot > Main Form.

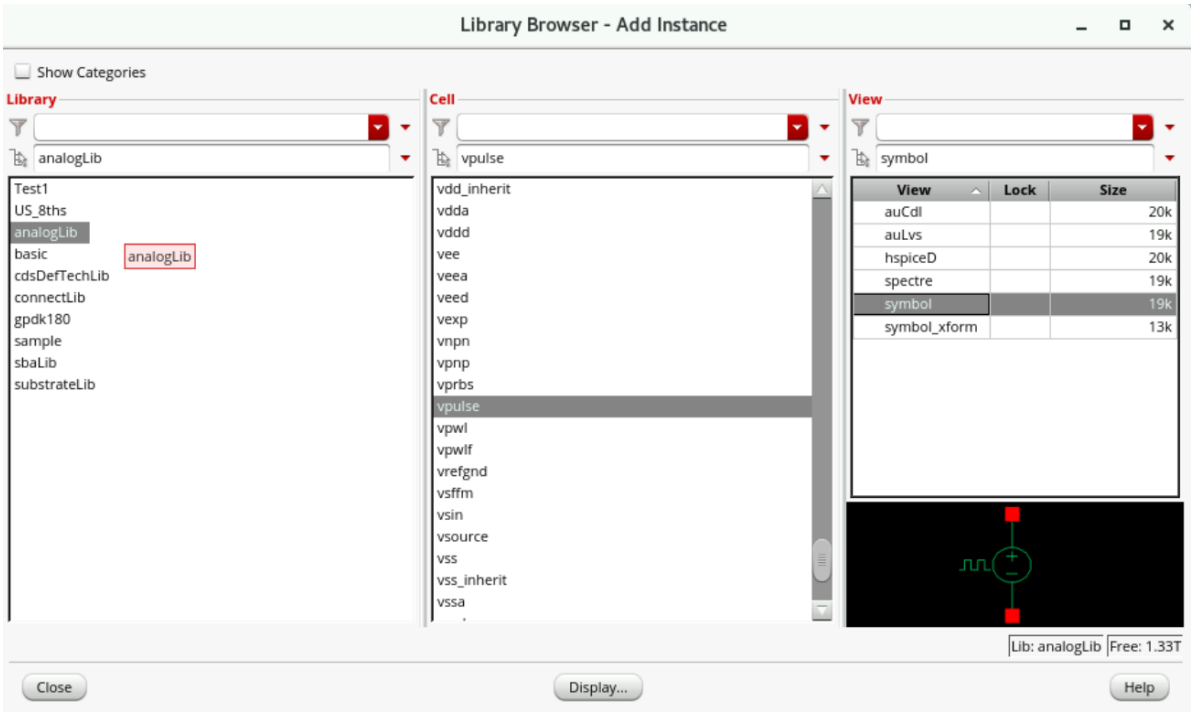
Alternatively, use the Results Browser to explore and manipulate the data.

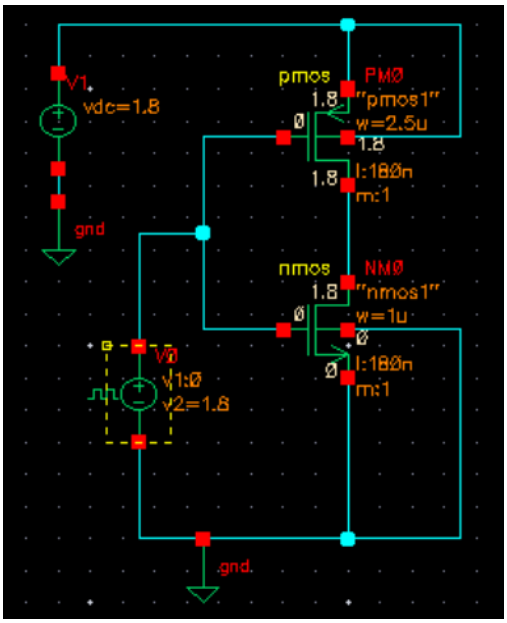
# Example: Inverter design and characterizing

## Test Bench Setup:

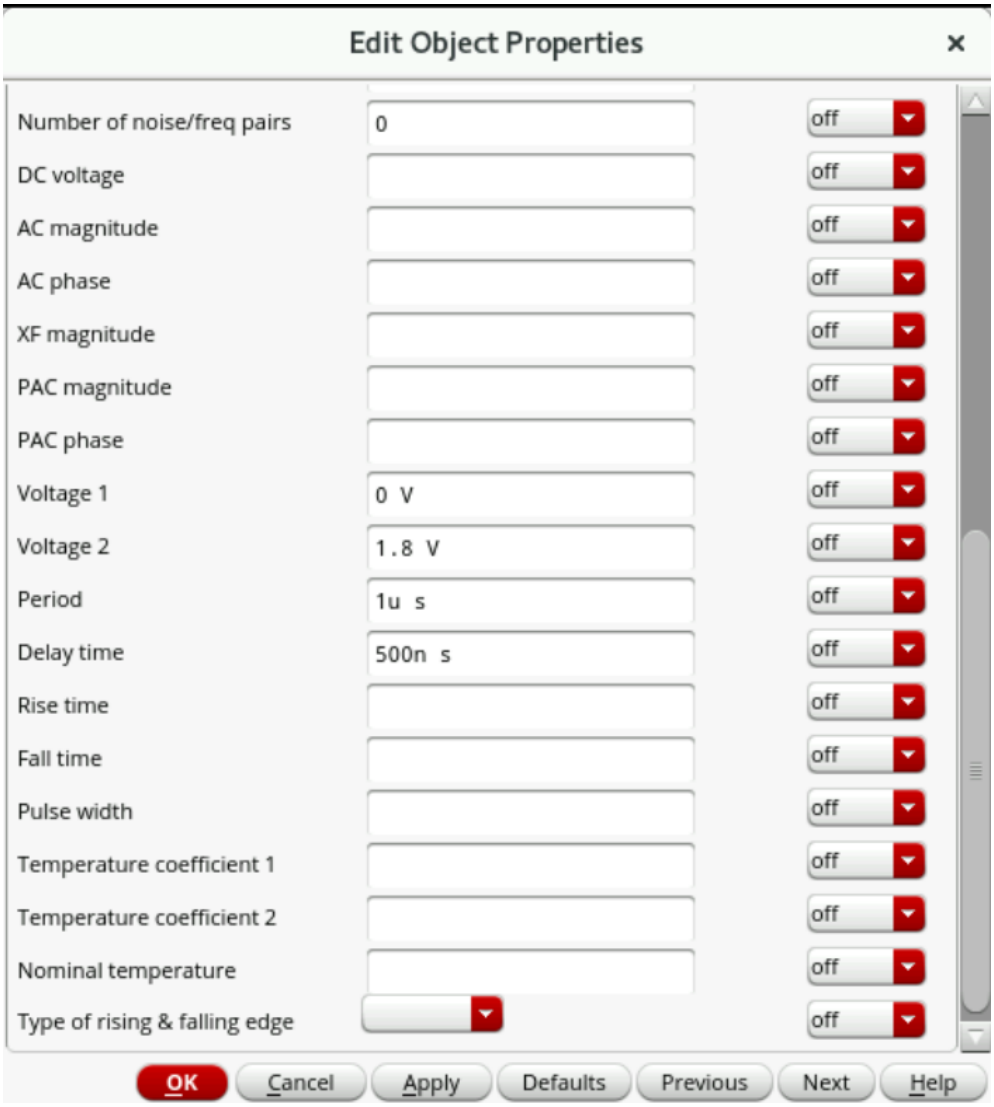
### a- Transient Analysis

Create a schematic like the following picture. You can add **vdc** source and **vpulse** from **analogLib** library.



Select **vpulse** component on schematic and then press '**Q**' for edit object properties:




Then do the same thing for the **vdc** source and set VDC value to 1.1V.

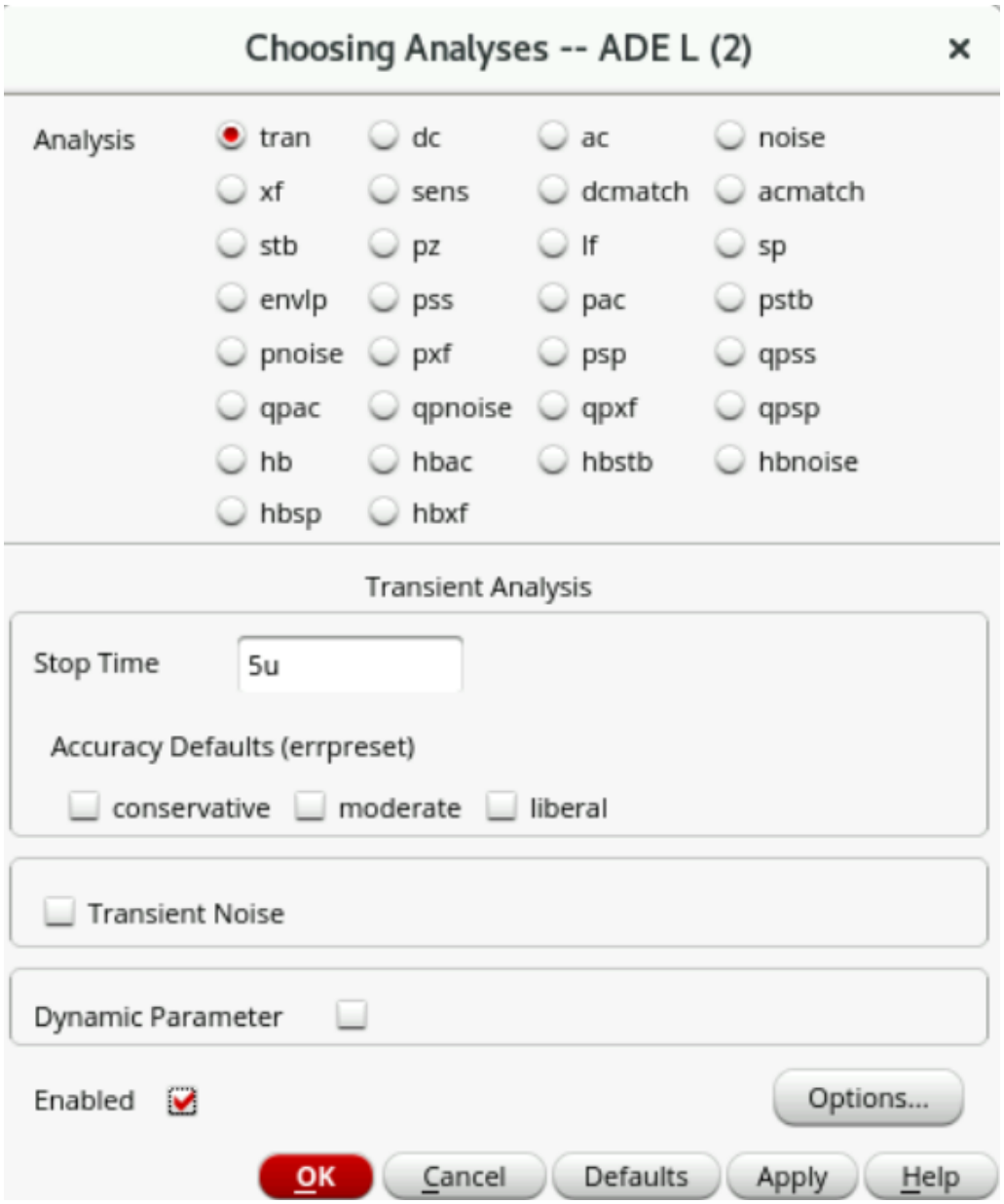
**Note:** The nominal VDD in gpdk45 technology is 1.1 V. So, you must set the VDD value to 1.1 V. Also, in vpulse you need to set high voltage to 1.1 V.

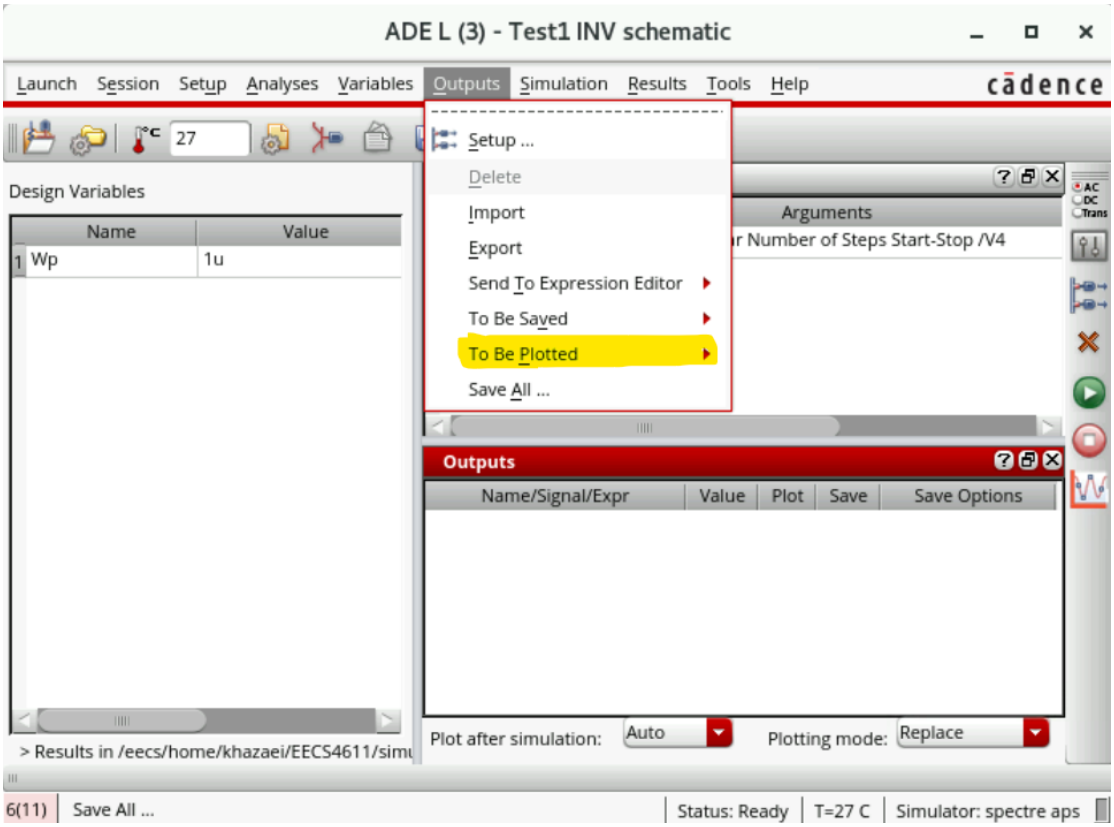
**Simulation Setup:**

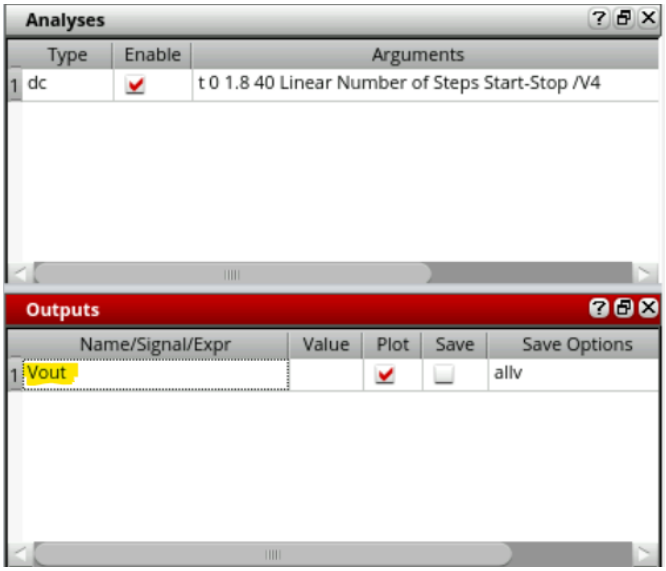
- ADE > Analyses > choose – Choose transient analysis and set stop time to reasonable value based on input pulse period.
- Select the outputs you want to plot after simulation (Outputs > to be plotted > select on design)

OR using Output > Direct Plot > Transient > Selecting on the schematic > press Esc (after running)

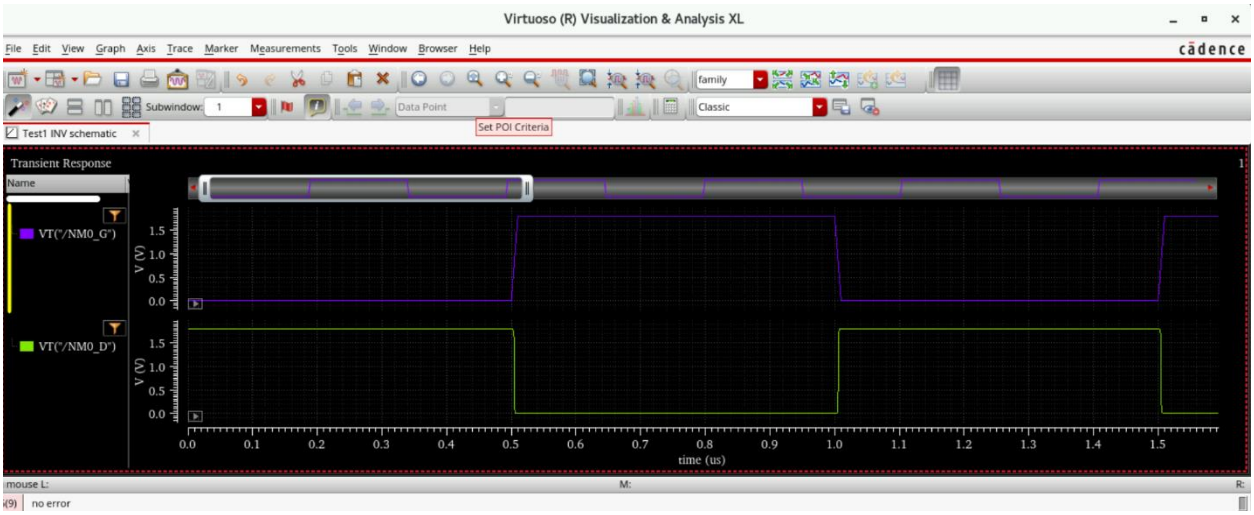
- **Run**




ADE L (3) - Test1 INV schematic
Launch Session Setup Analyses Variables Outputs Simulation Results Tools Help
cadence
Setup ...
Delete
Import
Export
Send To Expression Editor
To Be Saved
To Be Plotted
Save All ...
Design Variables
Name Value
1 Wp 1u
Arguments
r Number of Steps Start-Stop /V4
Outputs
Name/Signal/Expr Value Plot Save Save Options
Plot after simulation: Auto
Plotting mode: Replace
> Results in /eecs/home/khazaei/EECS4611/simu
6(11) Save All ...
Status: Ready T=27 C Simulator: spectre aps

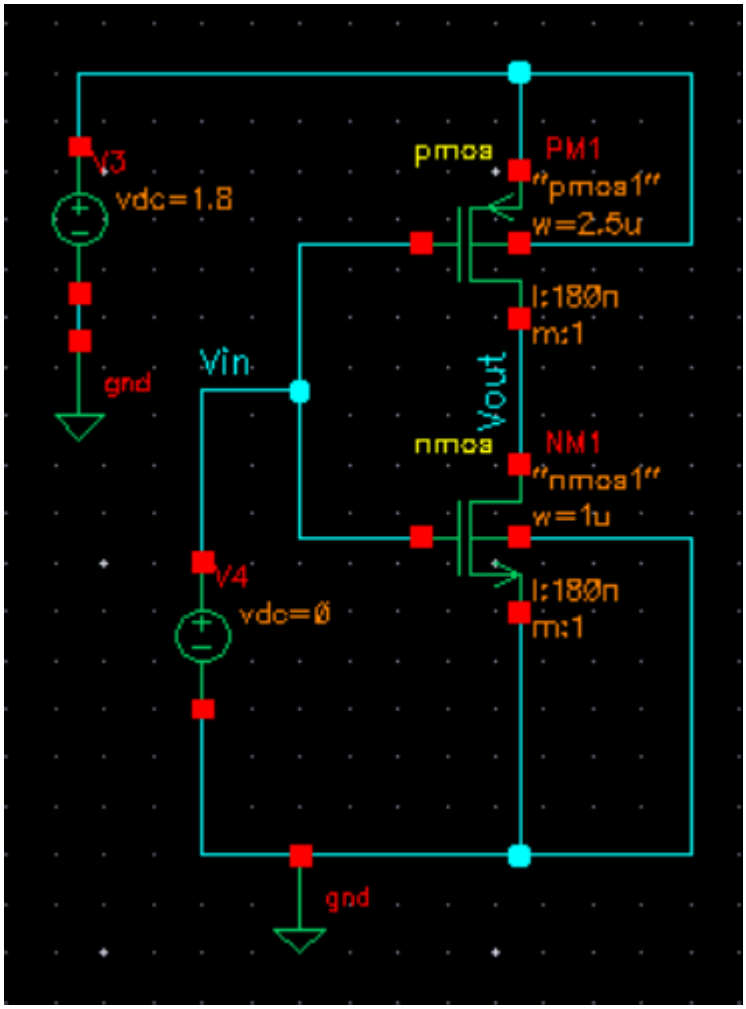

Analyses
Type Enable Arguments
1 dc t 0 1.8 40 Linear Number of Steps Start-Stop /V4
Outputs
Name/Signal/Expr Value Plot Save Save Options
1 Vout allv

Transient Result:

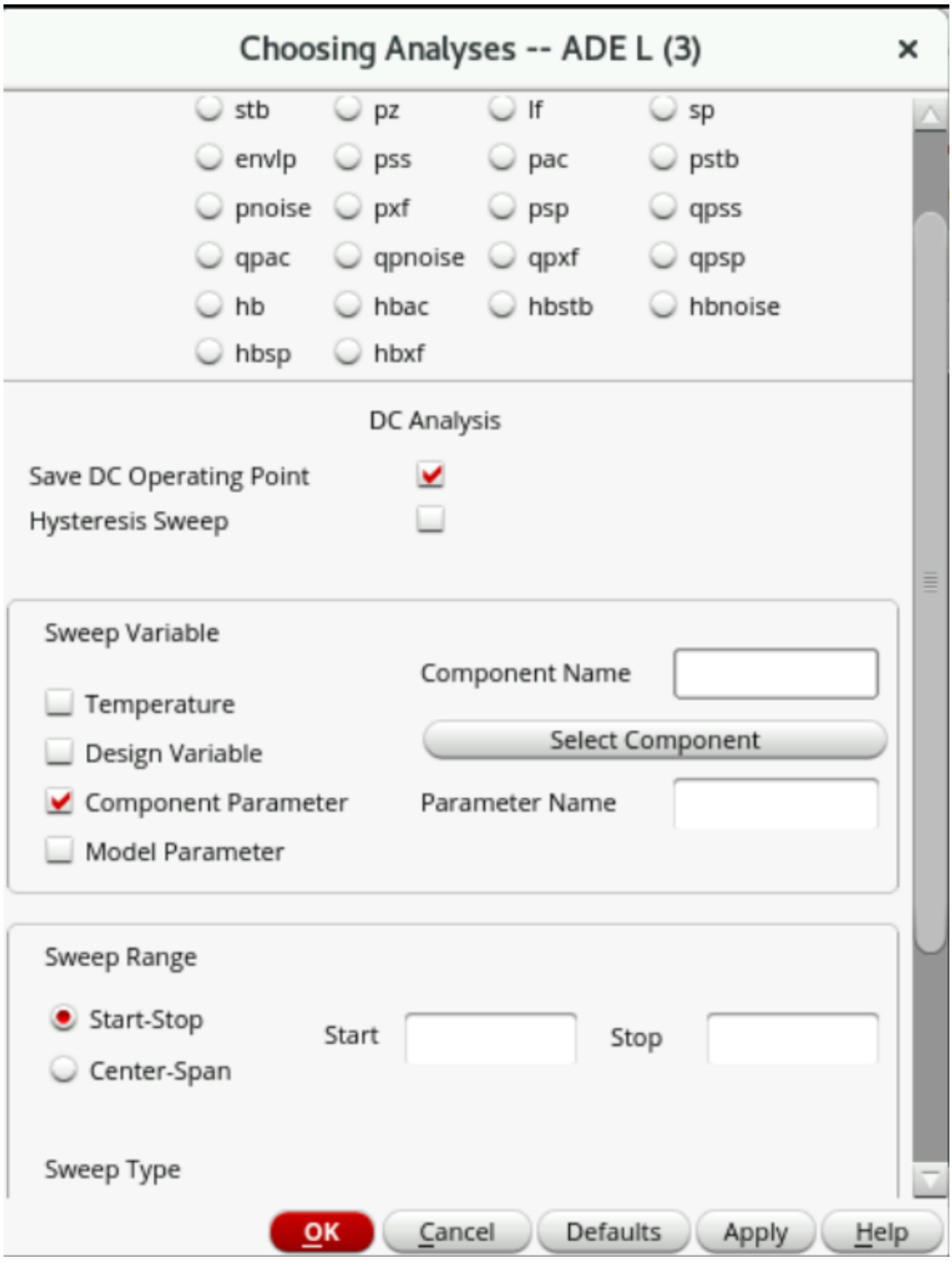


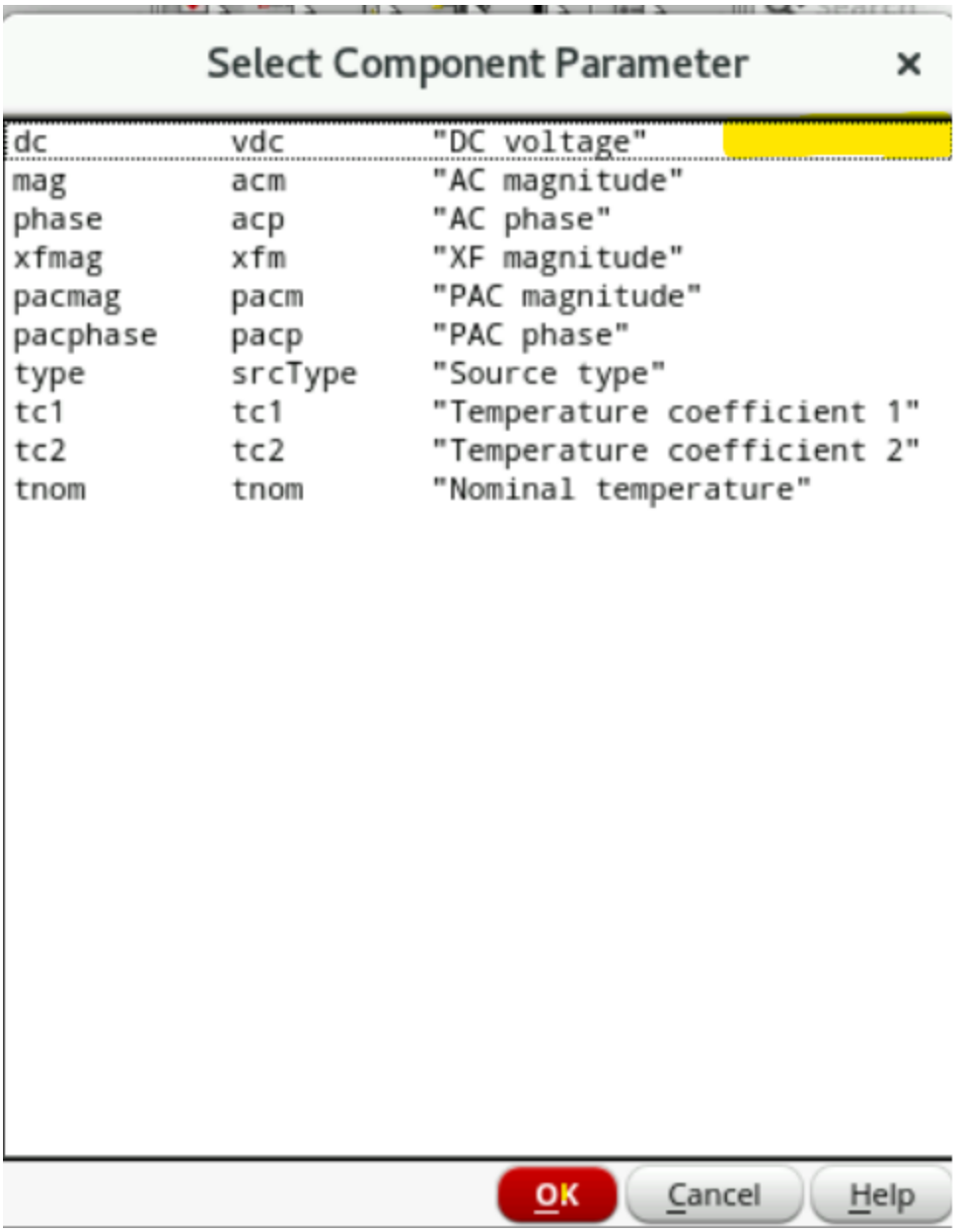
**b-Vin Sweep (Plotting Vout Vs Vin):**

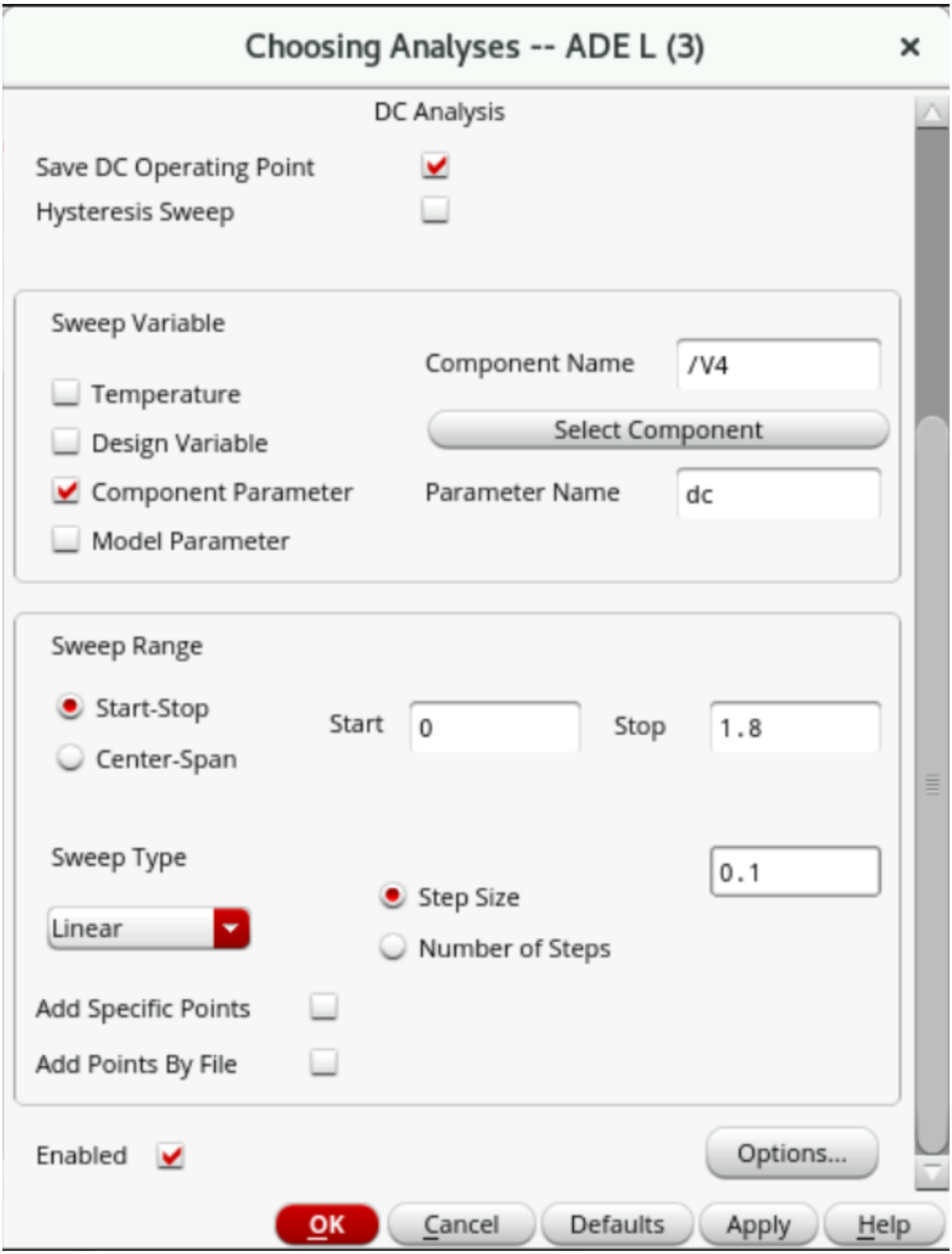
Test Bench Setup:



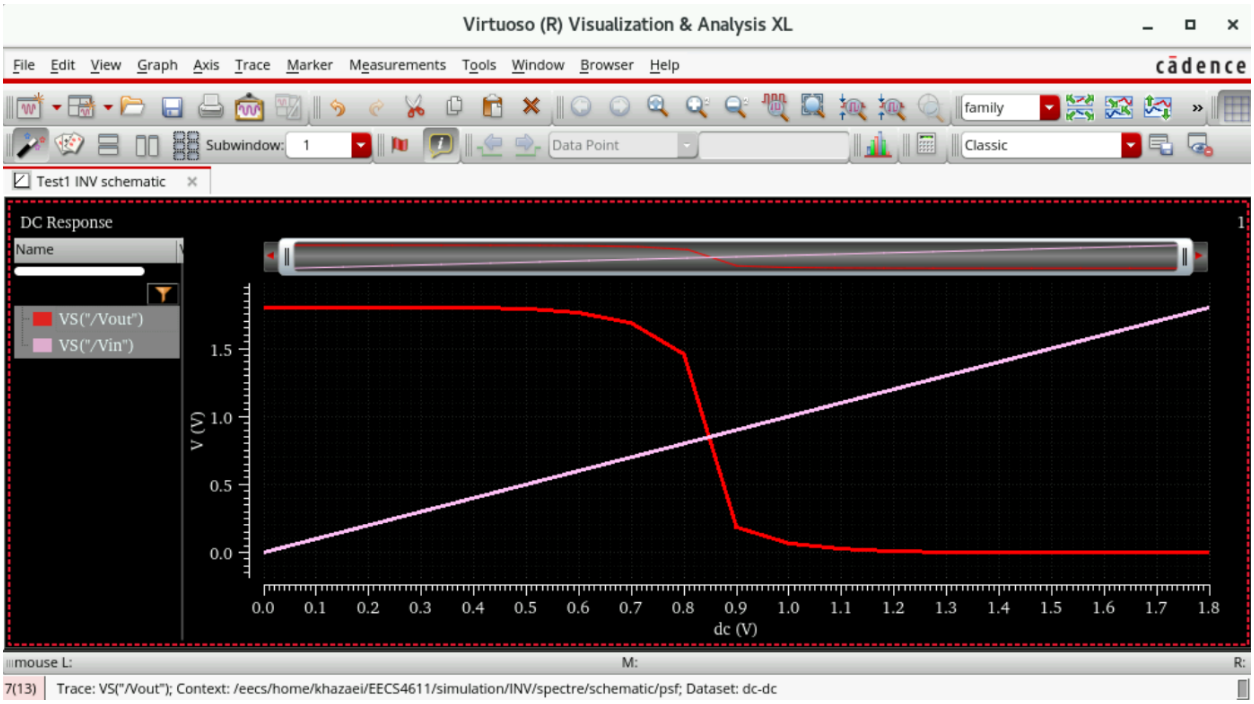

Set up a DC analysis and sweep Vin in the configuration menu (Select Component Parameter > Select Component > Click on “V4” Dc Voltage Source).


Choosing Analyses -- ADE L (3)
stb
pz
lf
sp
envlp
pss
pac
pstb
pnoise
pxf
psp
qpss
qpac
qpnoise
qpxf
qpsp
hb
hbac
hbstb
hbnoise
hbsp
hbxf
DC Analysis
Save DC Operating Point
Hysteresis Sweep
Sweep Variable
Component Name
Temperature
Select Component
Design Variable
Component Parameter
Parameter Name
Model Parameter
Sweep Range
Start-Stop
Start
Stop
Center-Span
Sweep Type
OK
Cancel
Defaults
Apply
Help


Select Component Parameter
dc vdc "DC voltage"
mag acm "AC magnitude"
phase acp "AC phase"
xfmag xfm "XF magnitude"
pacmag pacm "PAC magnitude"
pacphase pacp "PAC phase"
type srcType "Source type"
tc1 tc1 "Temperature coefficient 1"
tc2 tc2 "Temperature coefficient 2"
tnom tnom "Nominal temperature"
OK
Cancel
Help

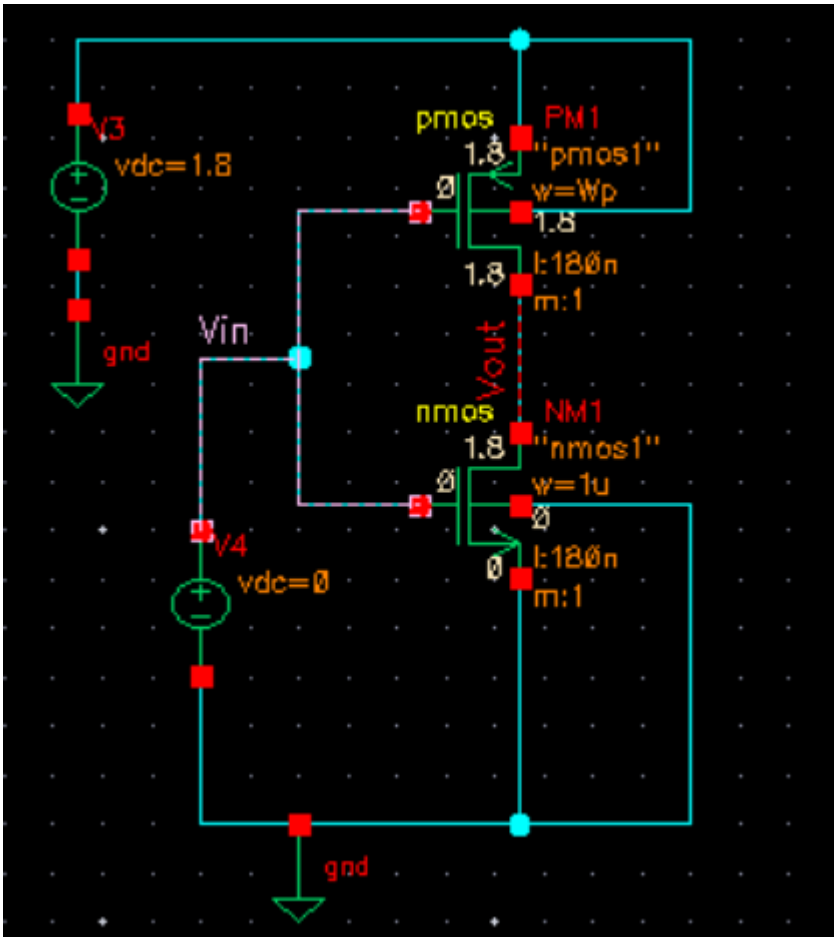

Choosing Analyses -- ADE L (3)
DC Analysis
Save DC Operating Point
Hysteresis Sweep
Sweep Variable
Component Name
/V4
Temperature
Select Component
Design Variable
Component Parameter
Parameter Name
dc
Model Parameter
Sweep Range
Start-Stop
Start
0
Stop
1.8
Center-Span
Sweep Type
0.1
Step Size
Linear
Number of Steps
Add Specific Points
Add Points By File
Enabled
Options...
OK
Cancel
Defaults
Apply
Help

Run.

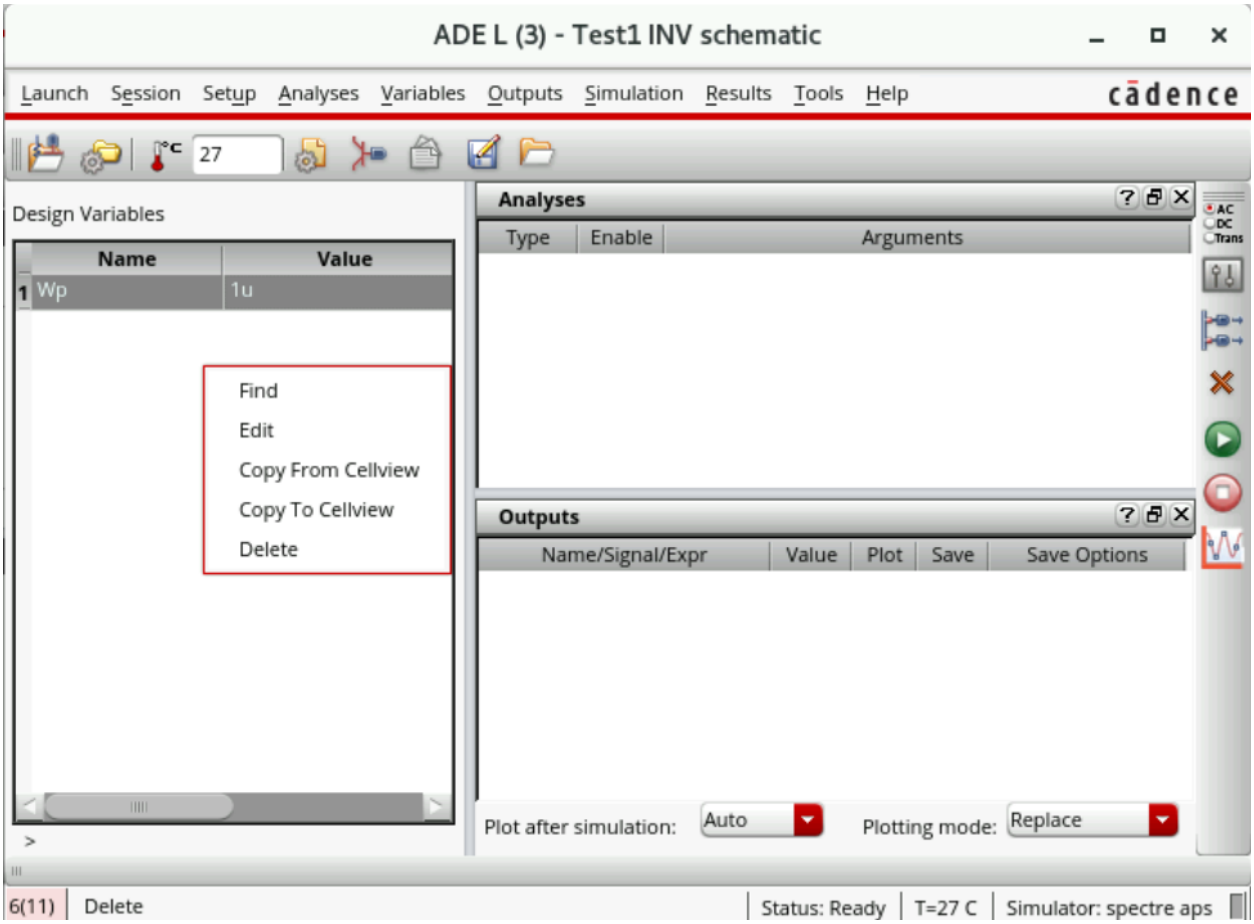

Virtuoso (R) Visualization & Analysis XL
File Edit View Graph Axis Trace Marker Measurements Tools Window Browser Help
cadence
family
Subwindow: 1
Data Point
Classic
Test1 INV schematic
DC Response
Name
VS("/Vout")
VS("/Vin")
V (V)
1.5
1.0
0.5
0.0
0.0 0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1.0 1.1 1.2 1.3 1.4 1.5 1.6 1.7 1.8
dc (V)
mouse L:
M:
R:
7(13)
Trace: VS("/Vout"); Context: /eecs/home/khazaei/EECS4611/simulation/INV/spectre/schematic/psf; Dataset: dc-dc

### c- Vin Sweep (Plotting Vout Vs Vin) + PMOS Transistor Width Sweep:

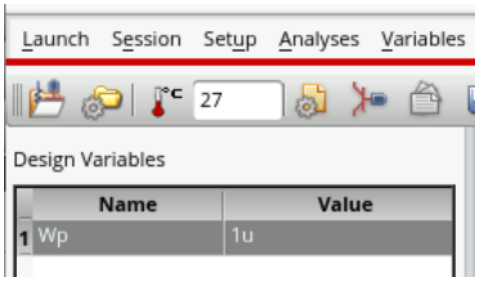
Setting up the schematic



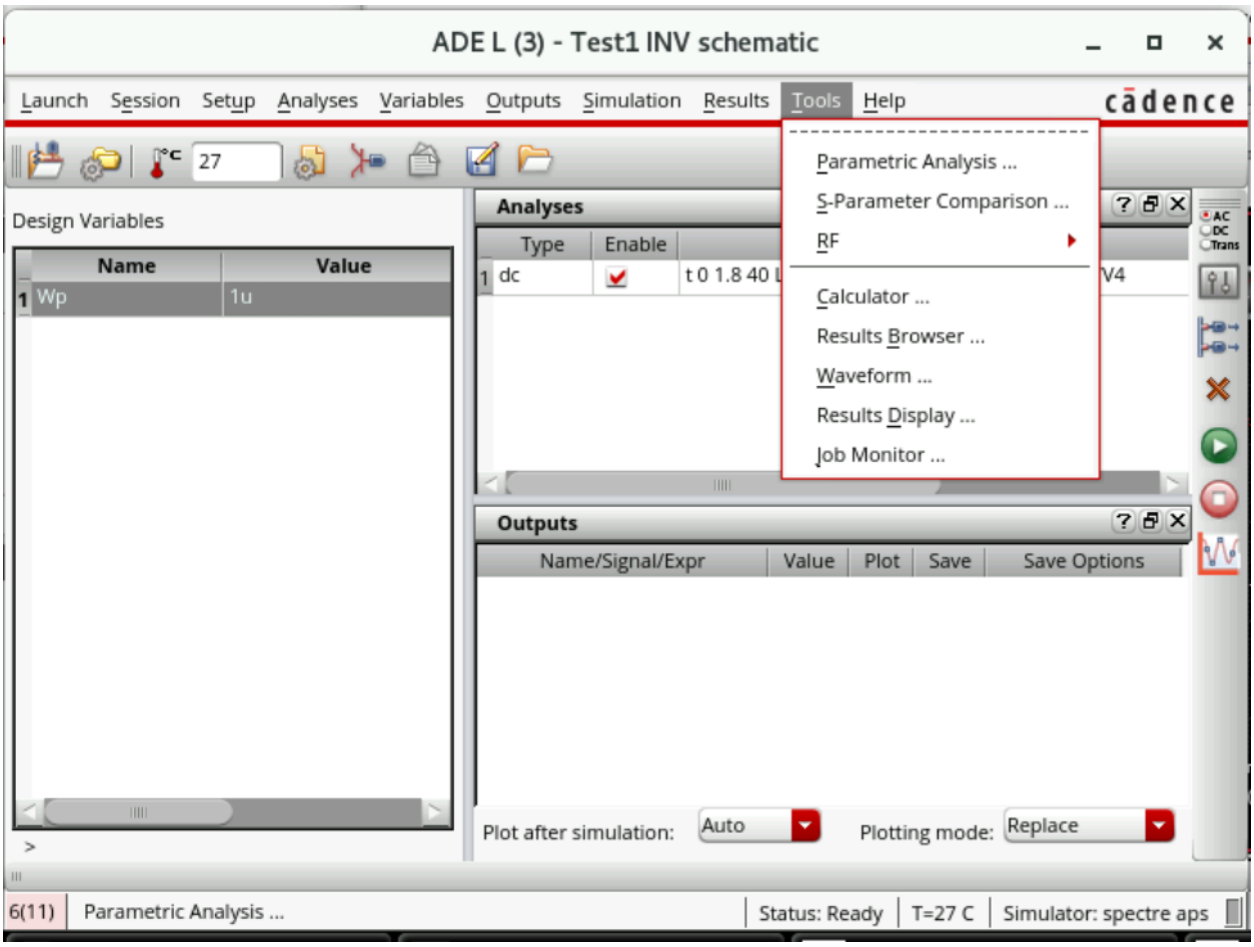
Inserting Wp variable: Right Click in the *Design Variable* window

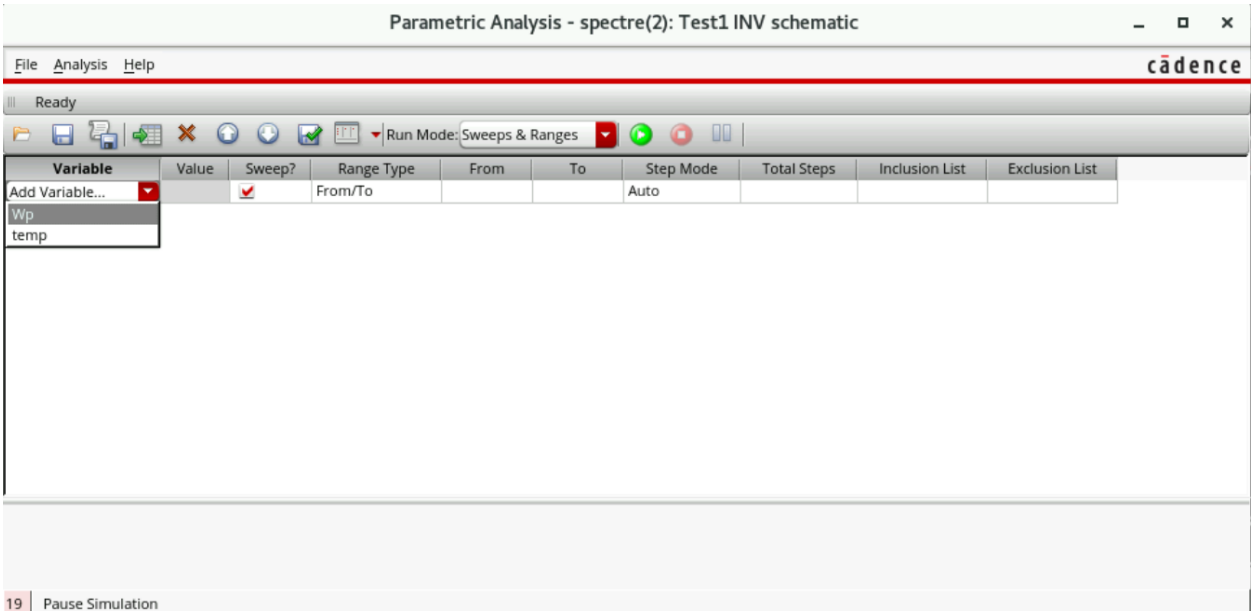


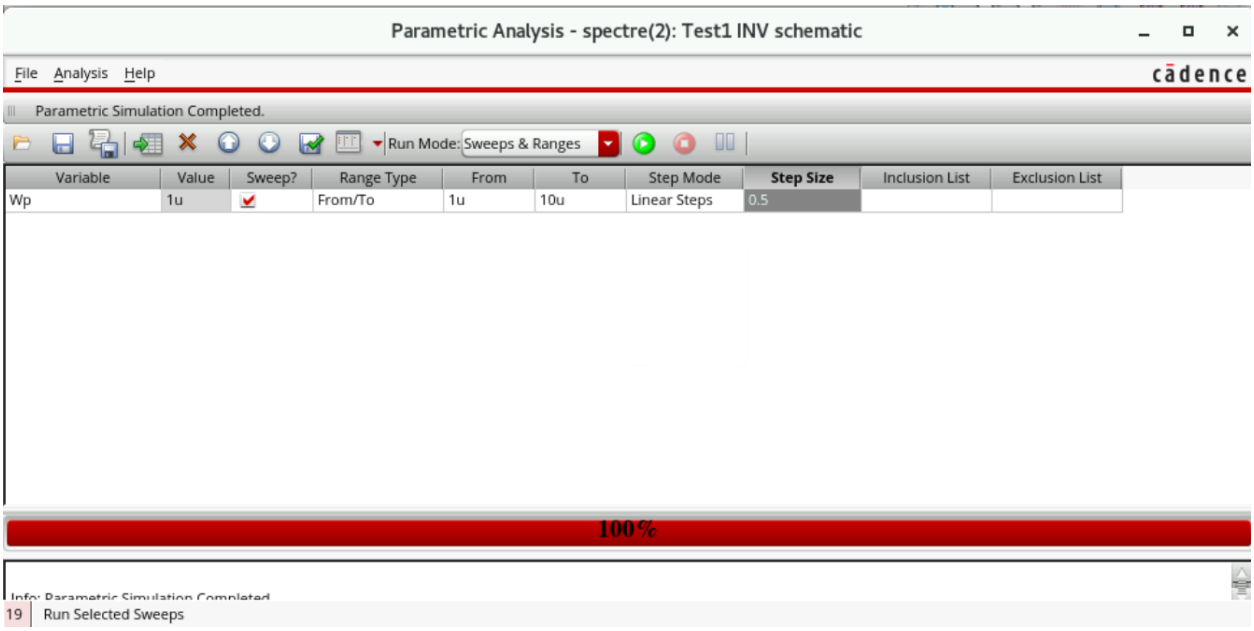

Copy From Cellview and import 1u as the initial value of the Wp variable.



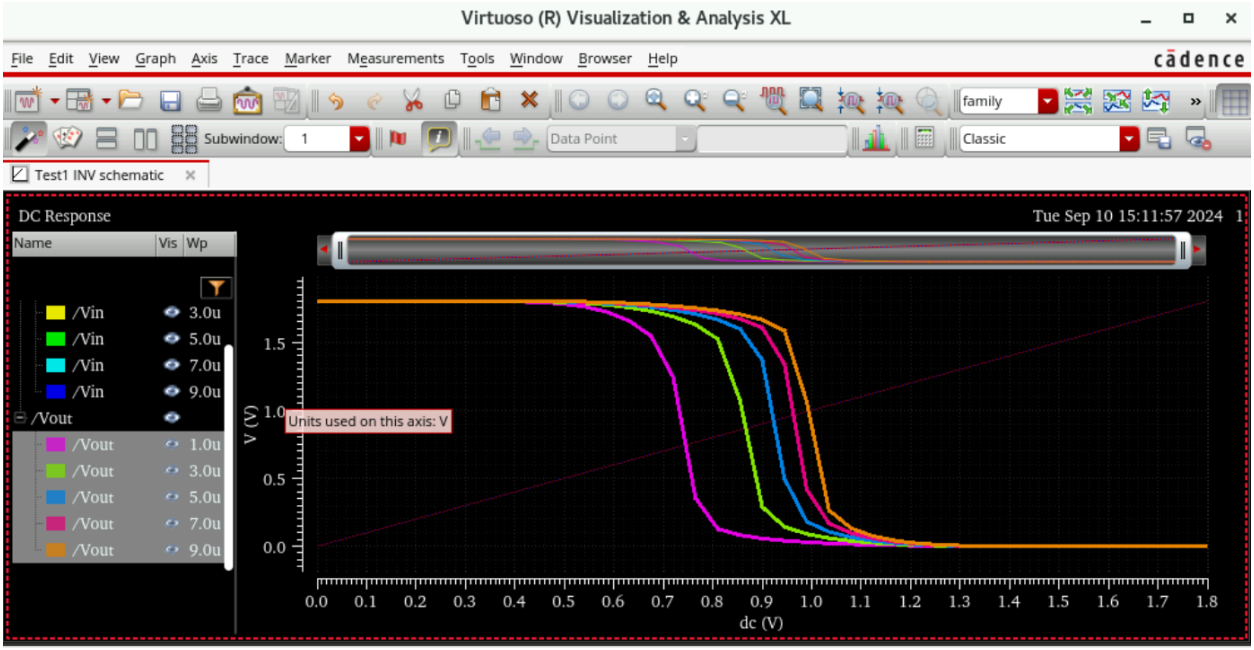
Sweep Wp (1um to 10um) from Tools > Parametric Analysis and Run





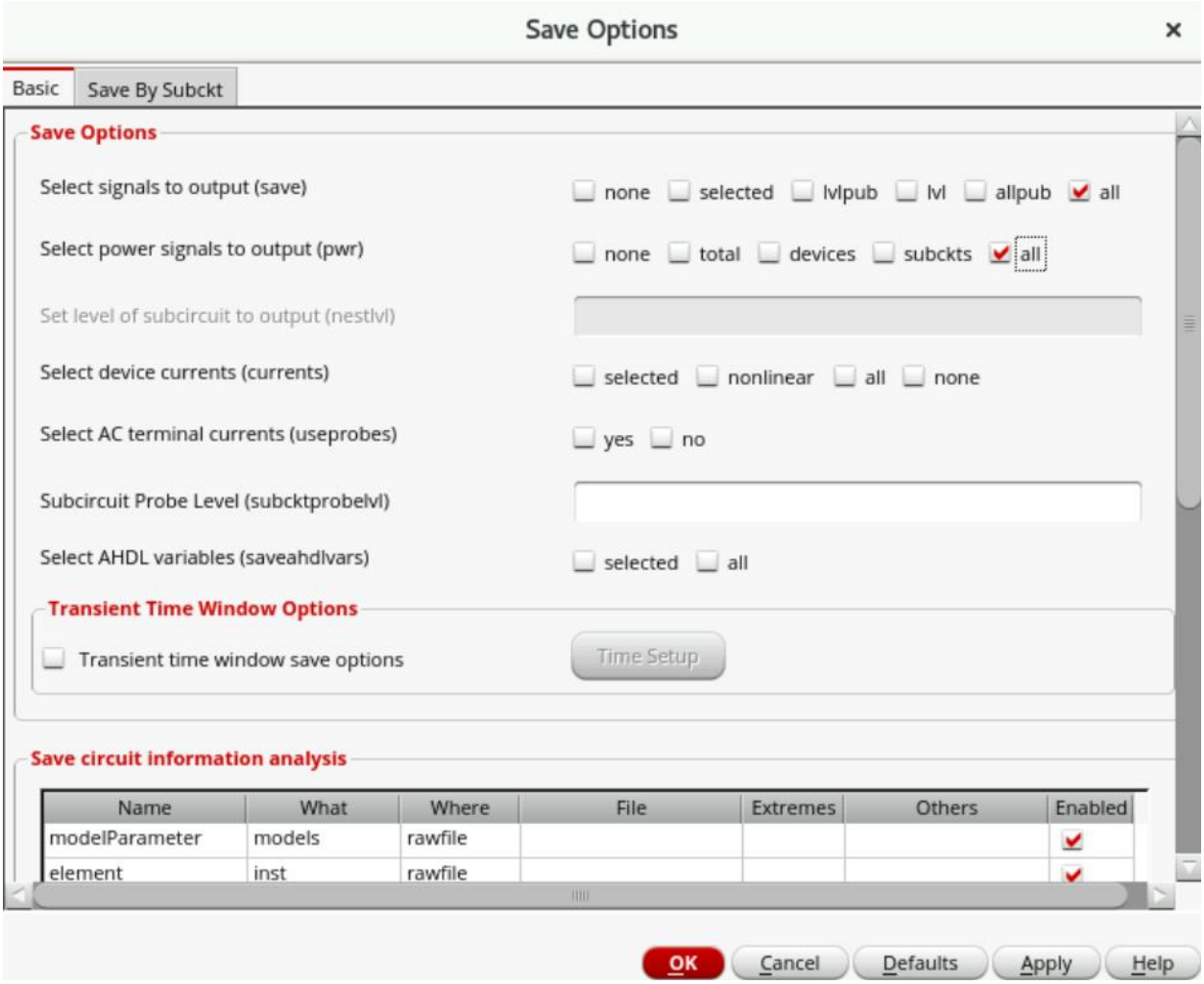

As the Vin and Vout are defined by setting the outputs (To be plotted) the figure will show output for Vin and Wp sweep.



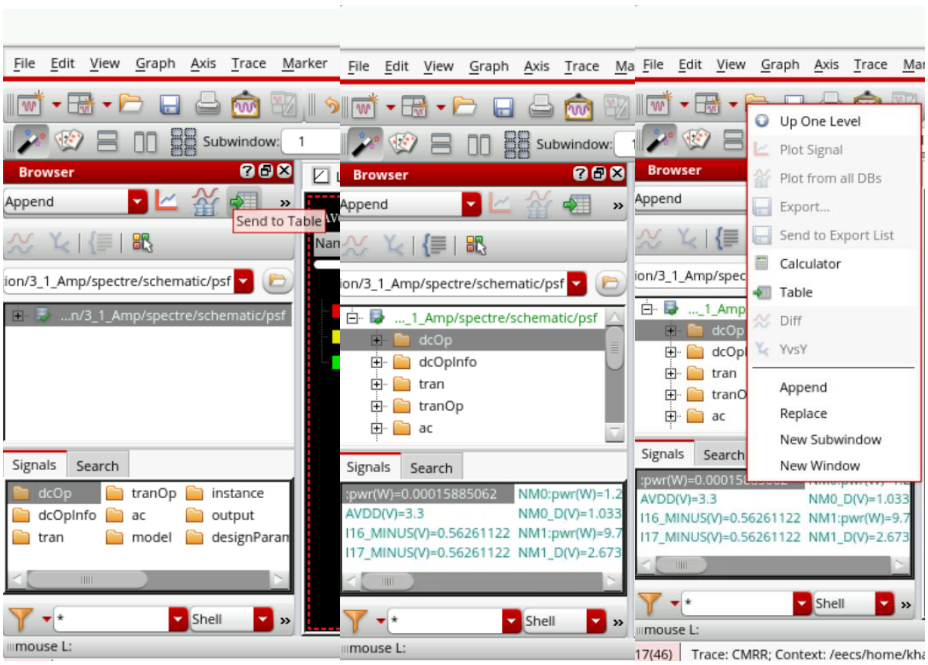
## Power Consumption

To evaluate the power consumption of a circuit in Cadence, it is essential to analyze both static and dynamic components to ensure optimal performance and efficiency. To do so, the following steps should be taken:

- Output > save all



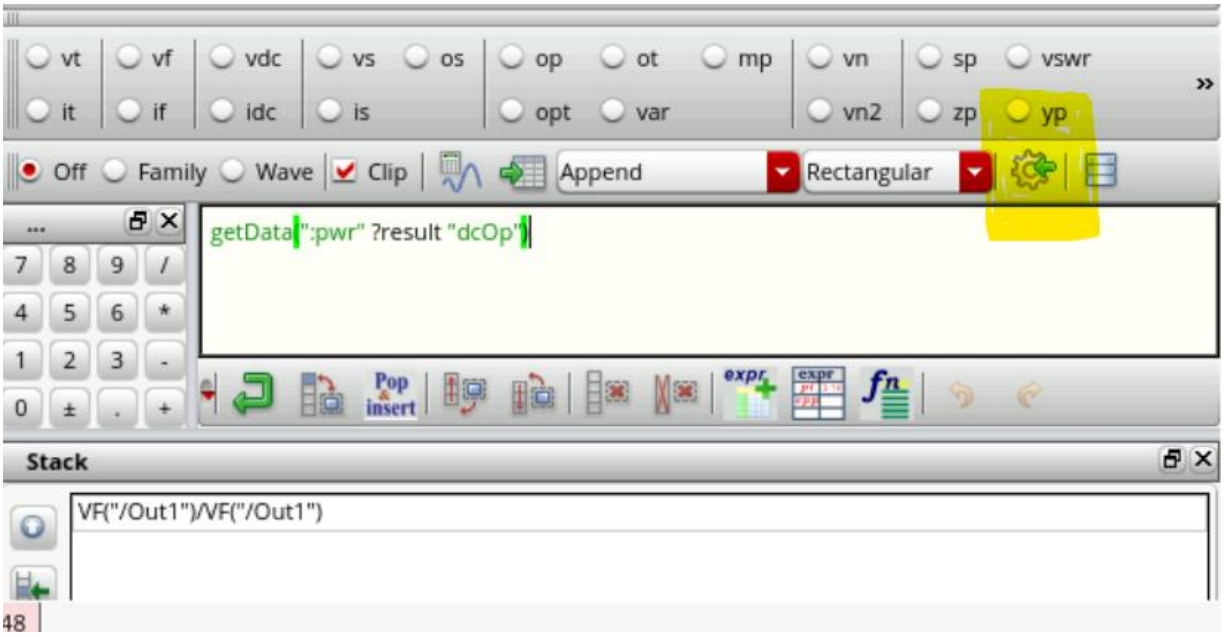

- Select all and apply.
- Run the simulation
- From the plotted figure follow **windows > Assistants > Browser**



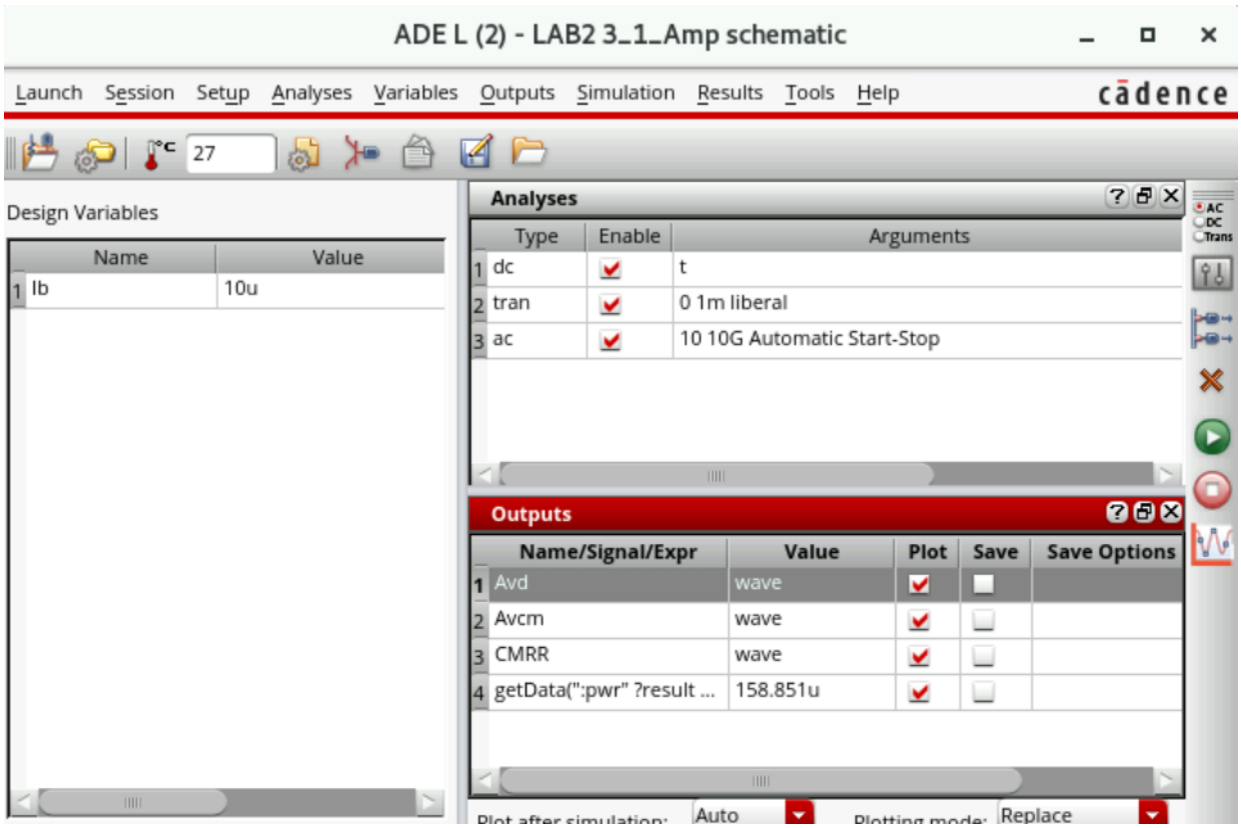

Select dcOp

Right click on pwr(W) > calculator

Send to ADL (Highlighted button)




Now, power consumption can be observed on ADE through any simulation.


ADE L (2) - LAB2 3_1_Amp schematic
Launch Session Setup Analyses Variables Outputs Simulation Results Tools Help
cadence
27
Design Variables
Name Value
1 Ib 10u
Analyses
Type Enable Arguments
1 dc t
2 tran 0 1m liberal
3 ac 10 10G Automatic Start-Stop
Outputs
Name/Signal/Expr Value Plot Save Save Options
1 Avd wave
2 Avcm wave
3 CMRR wave
4 getData(":pwr" ?result ... 158.851u
Plot after simulation: Auto
Plotting mode: Replace

## Drawing a Layout

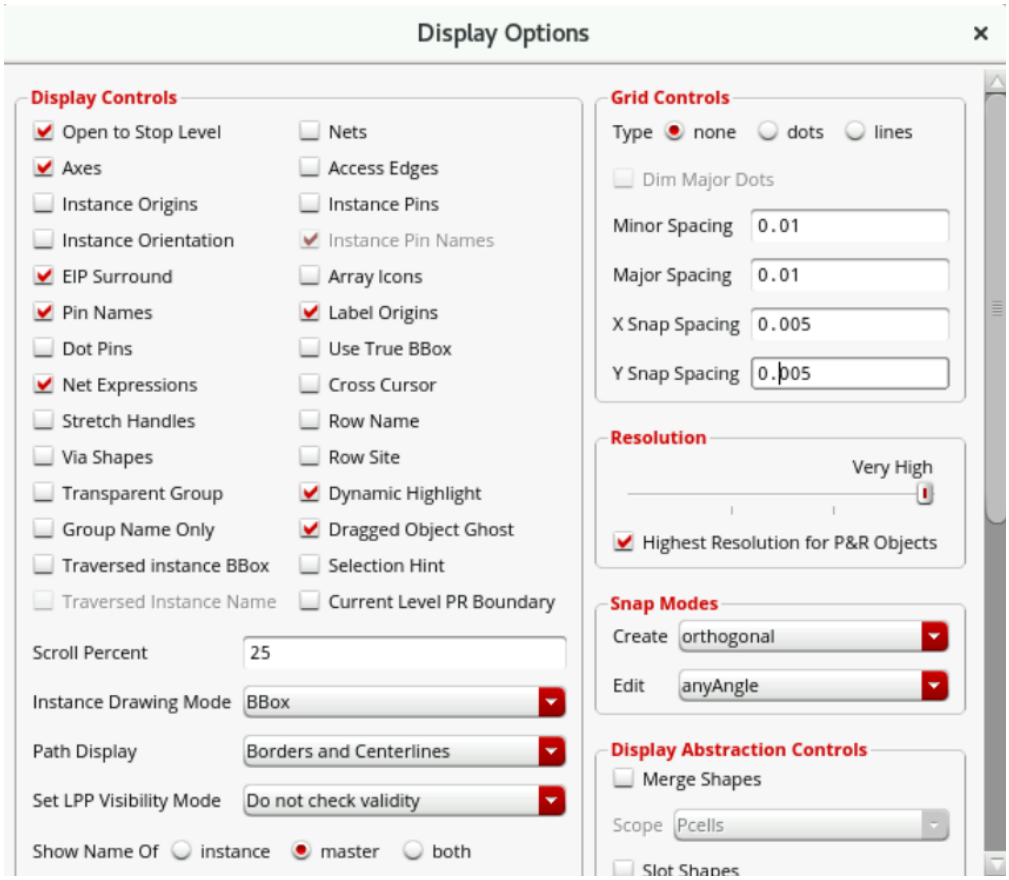
### Create a Layout:

In the schematic: Lunch > Layout XL

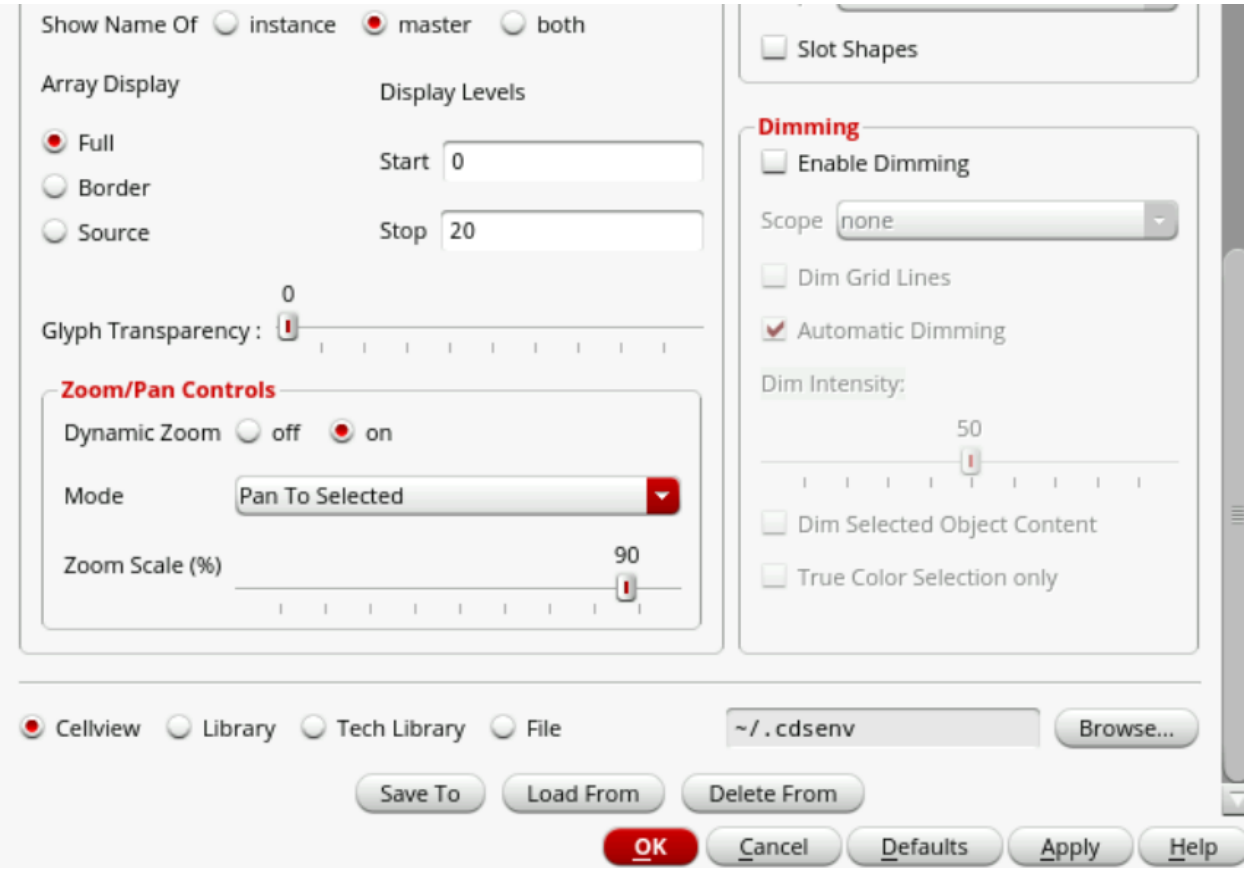
Or in the Library Manager, select your library and create a new cell view, choosing layout as the view type.

### Display Option:

Press “E” and change display option as:




**Note:** for the gpdk45 set Minor spacing = 0.001, Major Spacing = 0.005, X Snap Spacing = 0.001 and Y Snap Spacing = 0.001.




**Add Instances:**

Place transistors and other components in the layout editor using Create > Instance.

Or select the components from the schematic using Connectivity > generate > Selected from Source and click on the instance in the schematic view.

**Draw Metal Layers:**

Use Create > Shape > Path to draw metal connections. First, select metal1 in the LSW window, and adjust the width with Q.

**Run DRC/LVS (Design Rule Check and Layout vs. Schematic):**

Verify your layout using Pegasus > Run DRC and Run LVS to ensure it follows design rules.