Lab2 Circuit Simulation Using Cadence

Introduction

The objectives of this lab are to learn how to use Cadence tool to design a circuit and to analysis circuit using DC, AC, transient simulations. The CMOS process used in this lab is TSMC 0.18um technology, which is the same as in Lab1. There are ***two exercises*** in this lab.

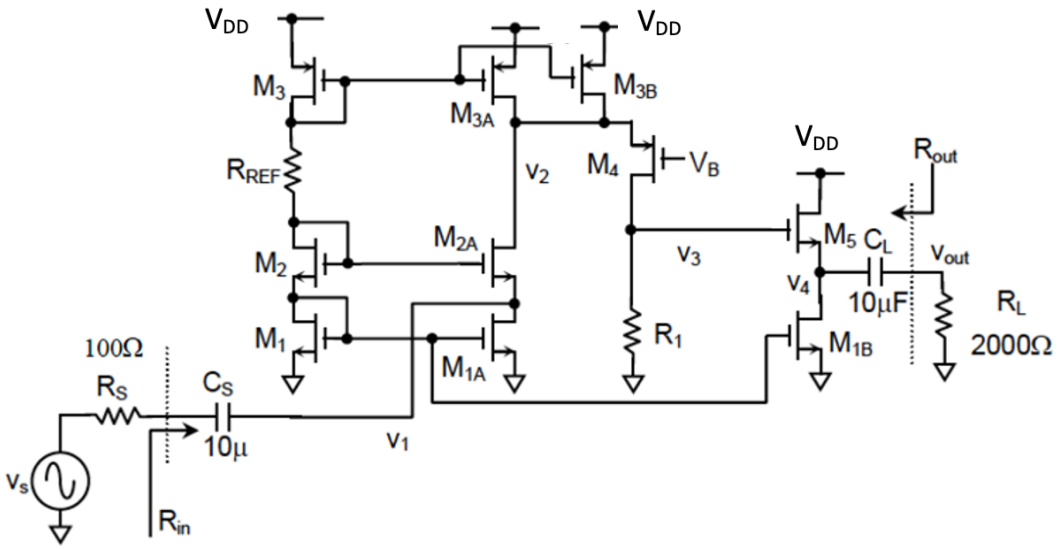
You need to submit a lab report that consists of following sections:

1. Introduction: a brief statement (few sentences) mentioning what you did in the lab and your results.
2. Equipment: please list equipment and software used in the lab.
3. Results and discussion: this is the main part of your lab report. Please include schematics used in each exercise, screen capture of important results, settings and plots for simulations. If you were asked to compare experimental results to the calculations, or to explain parts of your experiment, it should be presented in this section.
4. Conclusion: state what you learn from this lab, lab objectives you achieved, and any difficulties you met.

Lab Exercise 1

A multi-stage amplifier is given below, which is similar to Q2 in Assignment 5. In Assignment 5, you perform hand calculations to determine R_{REF} and R_1 based on drain current of M1-M3 and the overall gain, respectively. In this exercise, we use Cadence tool to determine R_{REF} and R_1. Assume that V_{DD}=2V, V_B=1V.

Please use “nmos2v” and “pmos2v” from tsmc18 library for all transistors when you create schematic for this circuit. Note “nmos2v” and “pmos2v” are cell names in tsmc18 library. For each transistor, you just need to enter 5 parameters: l (length), w (width), total_width, Number of Fingers, and Multiplier (m). Use 1 for Number of Fingers for all transistors. Transistor (W/L) ratios are in the form of w*m/l, where w is width, m is Multiplier, and l is length. Below is the list of (W/L) ratio for all transistors: M_1=M_{1A}=M_{1B}=20u*12/500n, M_2=M_{2A}=20u*20/1u, M_3=M_{3A}=M_{3B}=20u*12/500n, M_4=20u*8/500n, M_5=20u*12/1u.



Create a schematic, save it for following questions.

For following questions, please refer to Cadence Instruction for Lab Exercise 1 Section for detailed steps.

Q1. What is the value of R_{REF} such that the drain currents of M_1, M_2, and M_3 are 500uA.

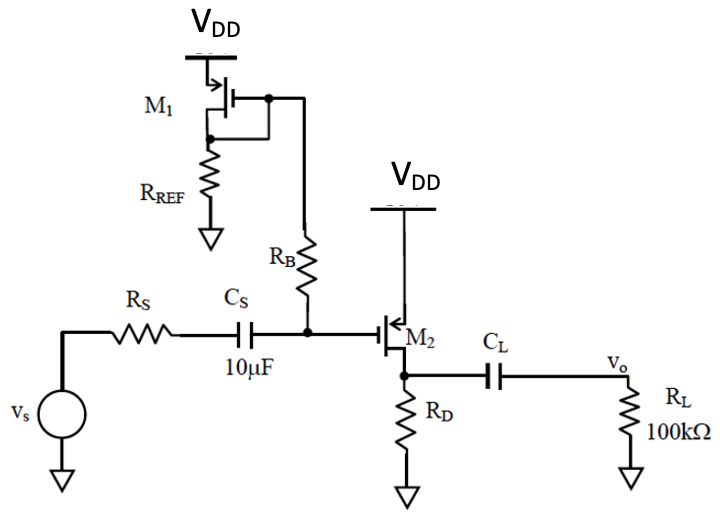
Q2. What is the value of R_1 such that the overall gain is 6. Verify that overall gain is 6 after you select the value of R_1.

Q3. Assume input is a sinusoidal with frequency of 1 MHz and peak-to-peak amplitude of 100mV, perform transient simulation to obtain DC biasing points at each node as well as the output waveform. After the simulation is completed, you should observe the DC biasing points at each node. Comments on the output waveform. Is the output waveform acceptable?

Q4. Suggest a simple fix on the circuit to solve the issue identified in Q3. Repeat the transient simulation to show that problem identified in Q3 is fixed. Please show the modified circuit and output waveform of modified circuit as well as your simulation setup.

Lab Exercise 2

Given the amplifier below, which is similar to Q1 of Assignment 4. In Assignment 4, you perform hand calculations to determine R_B and R_S based on f_U and C_L based on f_L. In this exercise, we use Cadence tool to determine R_B, R_S, and C_L.



Assume that V_{DD}=2V, R_B=100R_S, $R_{REF} = 4k\Omega, R_D = 4k\Omega,$ and the small signal AC gain is -1.6.

Please use "nmos3v" and "pmos3v" from tsmc18 library for all transistors when you create schematic for this circuit. Note "nmos3v" and "pmos3v" are cell names in tsmc18 library. For each transistor, you just need to enter 5 parameters: l (length), w (width), total_width, Number of Fingers, and Multiplier (m). Use 1 for Number of Fingers for all transistors. Transistor (W/L) ratios are in the form of w*m/l, where w is width, m is Multiplier, and l is length. Below is the list of (W/L) ratio for all transistors: $(W/L)_{M1} = 80u * 1/20u,\ (W/L)_{M2} = 160u * 1/10u.$

Create a schematic based on the given circuit using Cadence Virtuoso Schematic Editor, save your schematic.

For following questions, please refer to Cadence Instruction for Lab Exercise 2 Section for detailed steps.

Q1. What are the values of R_B and R_S such that the f_U is around 40MHz?

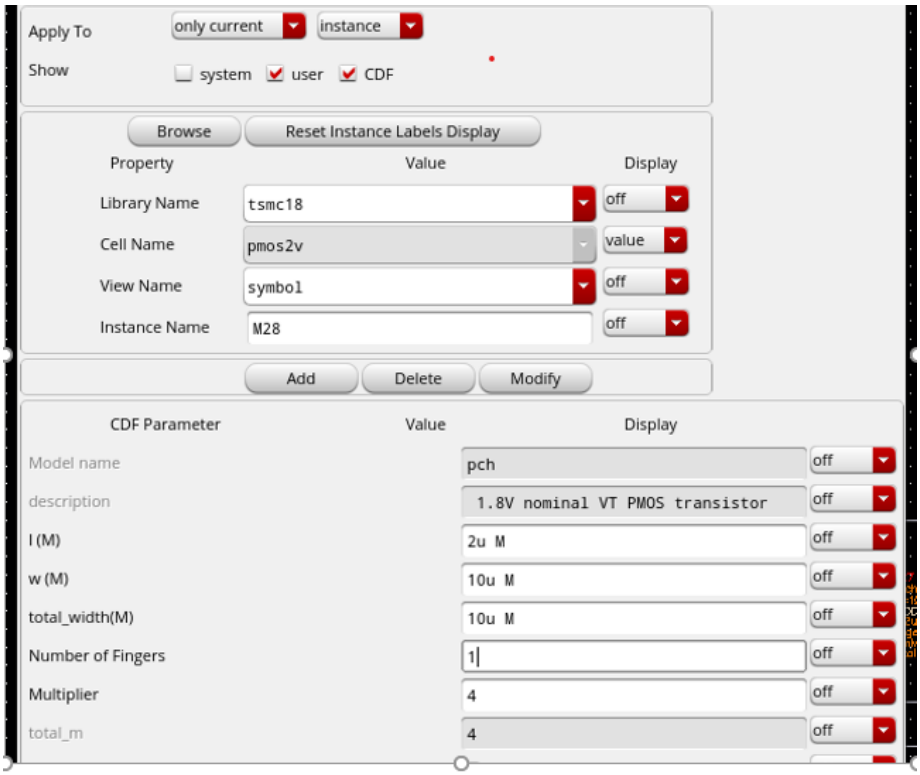
Q2. What is the value of C_L such that the f_L is around 50Hz?

Q3. Verify that the designed R_B, R_S, and C_L meet the design goal of f_U around 40MHz, f_L is around 50Hz, and overall gain around -1.6.

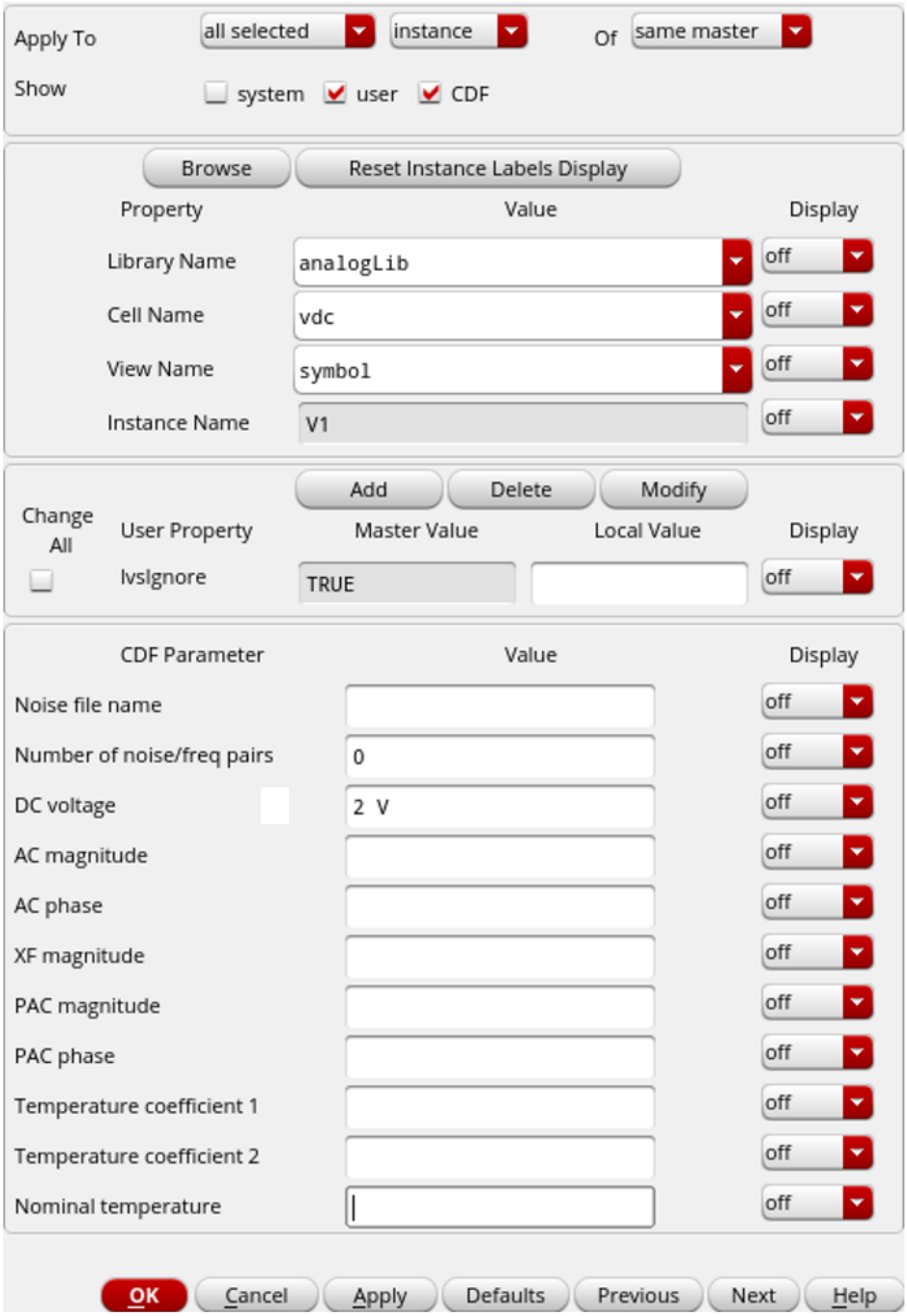
Cadence Instructions

Instructions for Lab Exercise 1.

1. Create a schematic based on the given circuit using Cadence Virtuoso Schematic Editor (detailed steps can be found in Lab1 instructions). After launch Schematic Editor, press shortcut key “i”, a window pops up for you to add a device. Below is an example on how to add a “pmos2v” device with (W/L)=10u*4/2u. For resistors and capacitors, you can get from “analogLib”, e.g. cells “res” and “cap”.

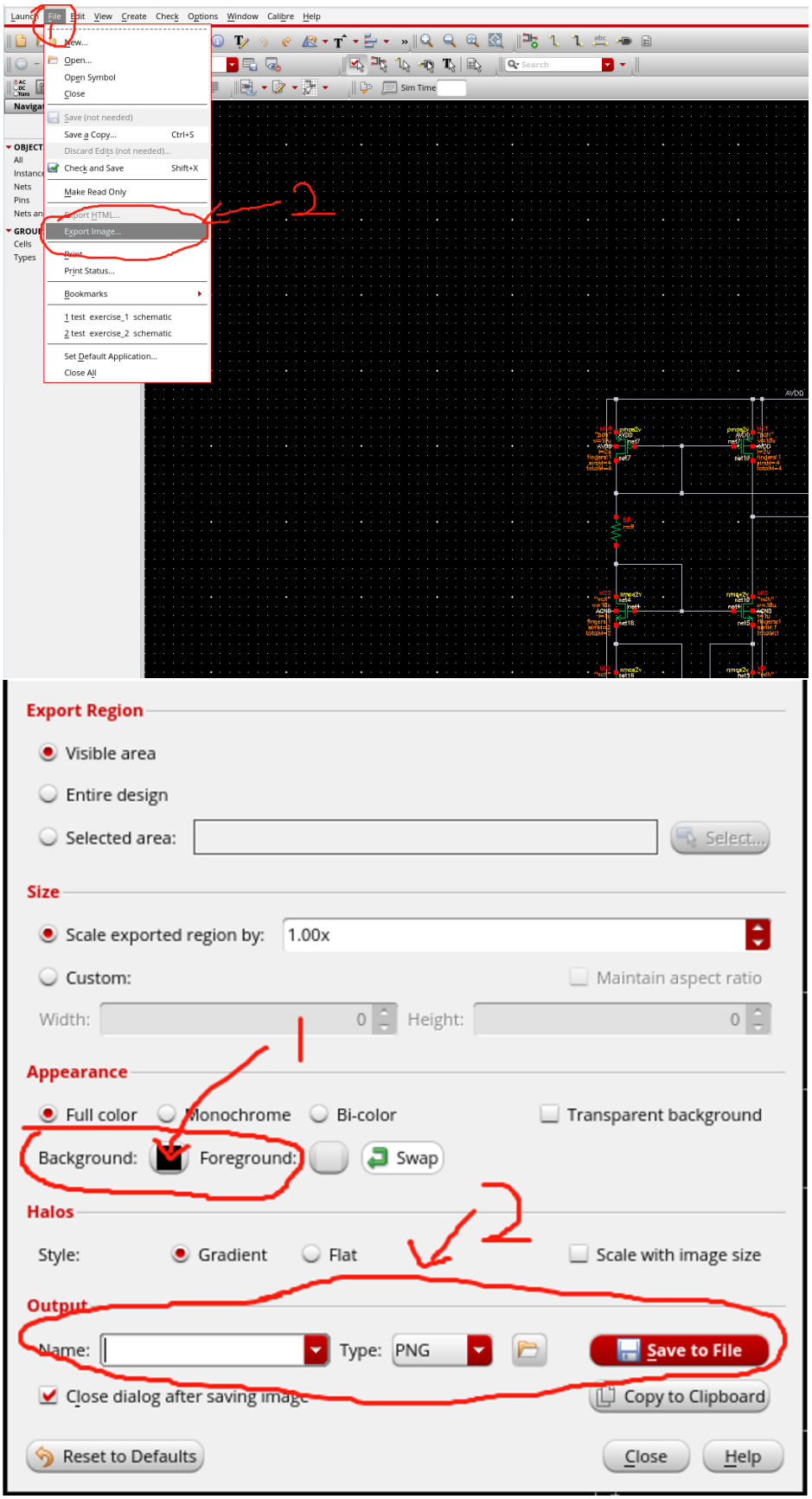


For DC supply, you need to “vdc” cell from "analogLib" in "Library". DC voltage values are 2 for a V_{DD} and 1 for V_B. For signal source Vs, we will add it later.



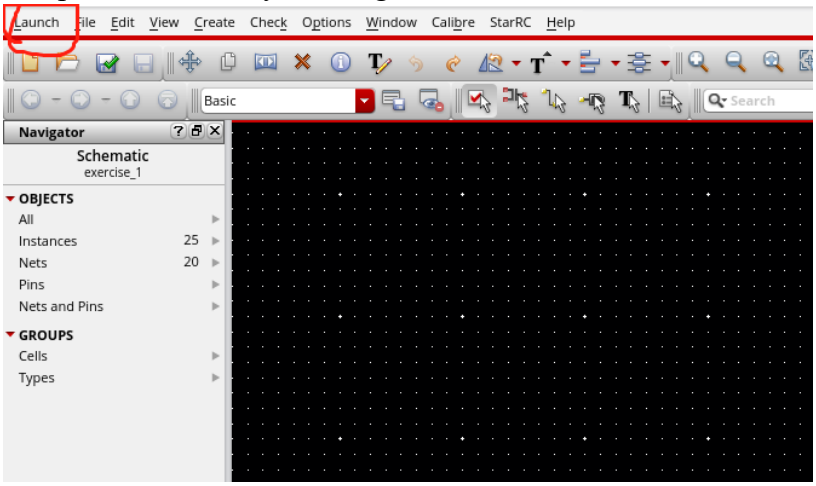
To capture a white background schematic, do the following:

a) Click on File, then Export image as shown Red circles 1 and 2 below. A window pops up.
b) In the pop-up window, set the background and foreground colors.
c) Specify the location to save your file.

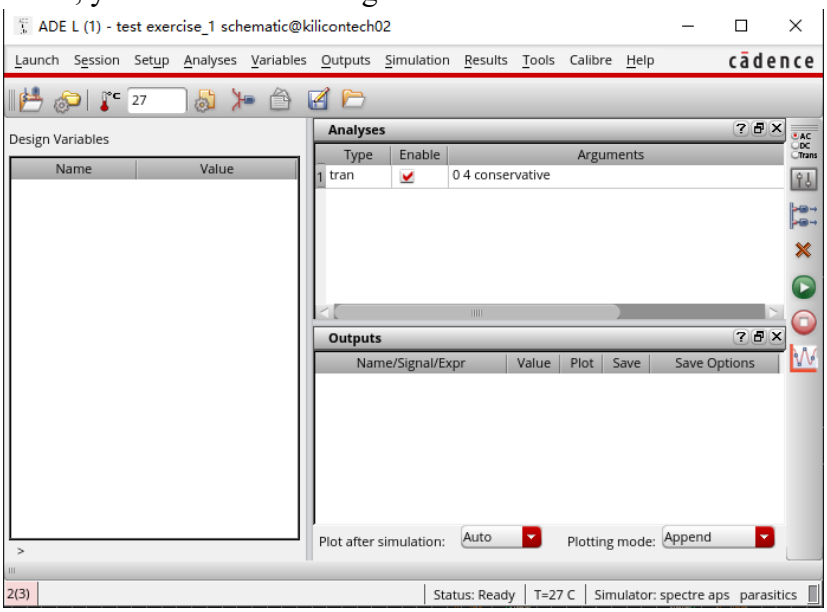


2. Make sure you have a supply voltage signal of 2V added during schematic creation.
3. Launch the ADE L Analog Design Environment from the Virtuoso Schematic

composer window by clicking on “Launch” as circled below.



Once you click on “Launch”, a drop-down menu shows. Select ADE L from the menu, you will see following ADE L window.



4. To set R_{REF} as a variable, select the resistor in your schematic then press the shortcut key “q”, a dialog box pops up. In the “Resistance” box, enter the variable “R” (Note a unit Ohms will automatically appear after entering R). The variable will be used in the following DC sweep simulation. Click "OK" to complete the setting as shown in Fig. 1.

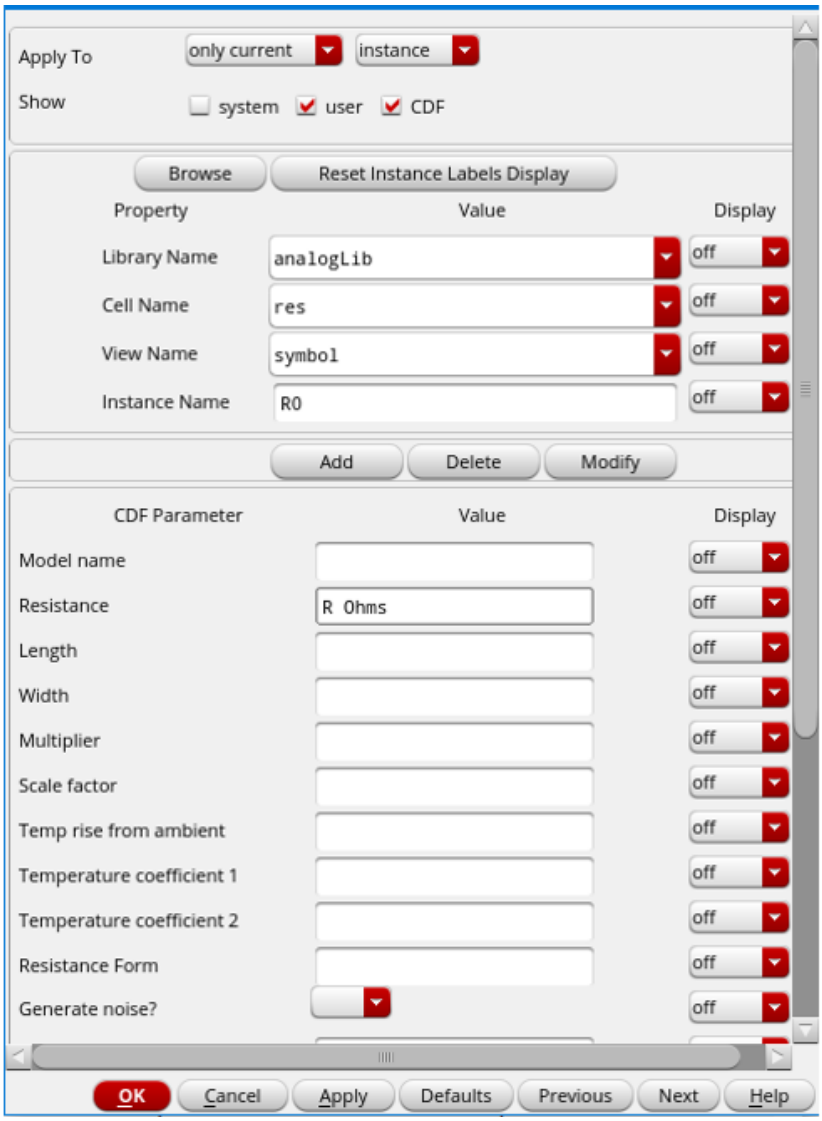


Fig. 1 R variable parameter setting

5. On ADE L window, select the "Variables"→ "Copy from Cellview", a dialog box of Design Variables you just set in above step will appear, you should set R as a random number. Select "Analyses"→"Choose" command in the ADE window, a dialog box pops up. Make the following selections in the box, "DC" and "Save DC Operating Point" under DC Analysis, "Design Variable" under the "Sweep Variable". A "Variable Name" option will appear on the right side of the dialog box, and you will need to right-click the "Select Design Variable" option to add the Variable Name. You also need to set a range for your variable in the "Sweep Variable". click "OK" Button to complete the setup as in Fig. 2.

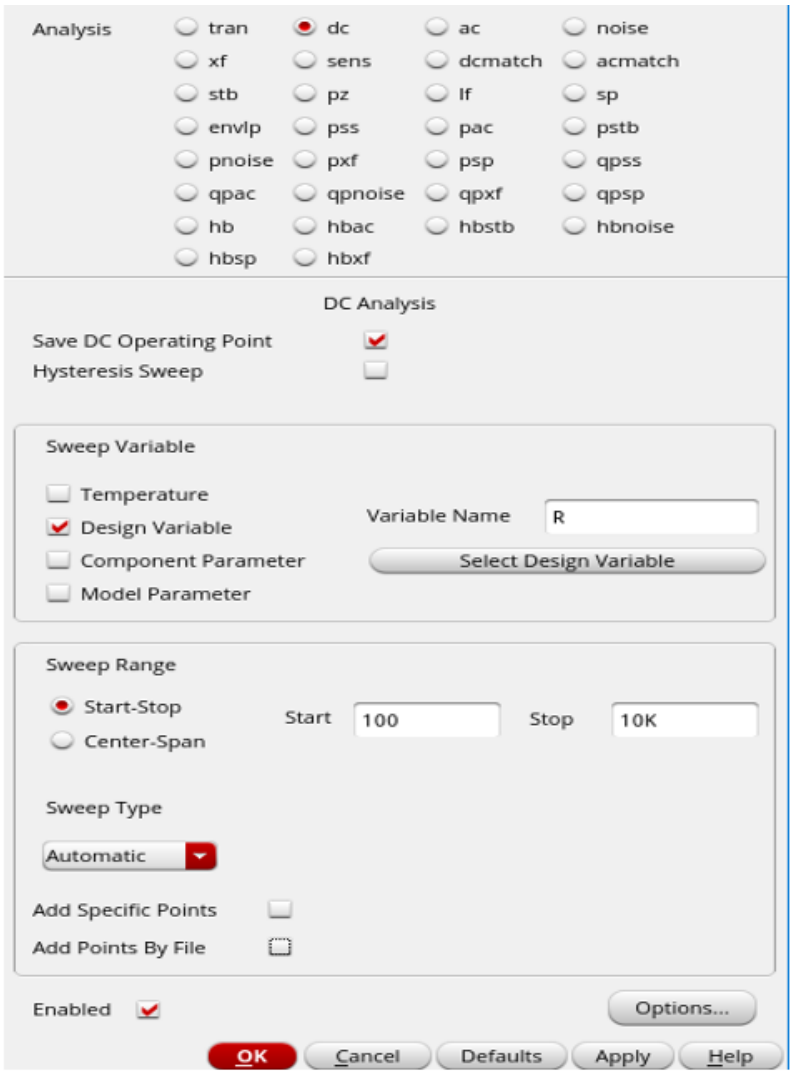


Fig. 2 DC simulation Configuration

6. Select "Outputs"→"To be saved"→"Select On Design", as shown in Fig.3, then return to your circuit to select the node you want to save the value. Press the "Esc" to terminate the selection process.

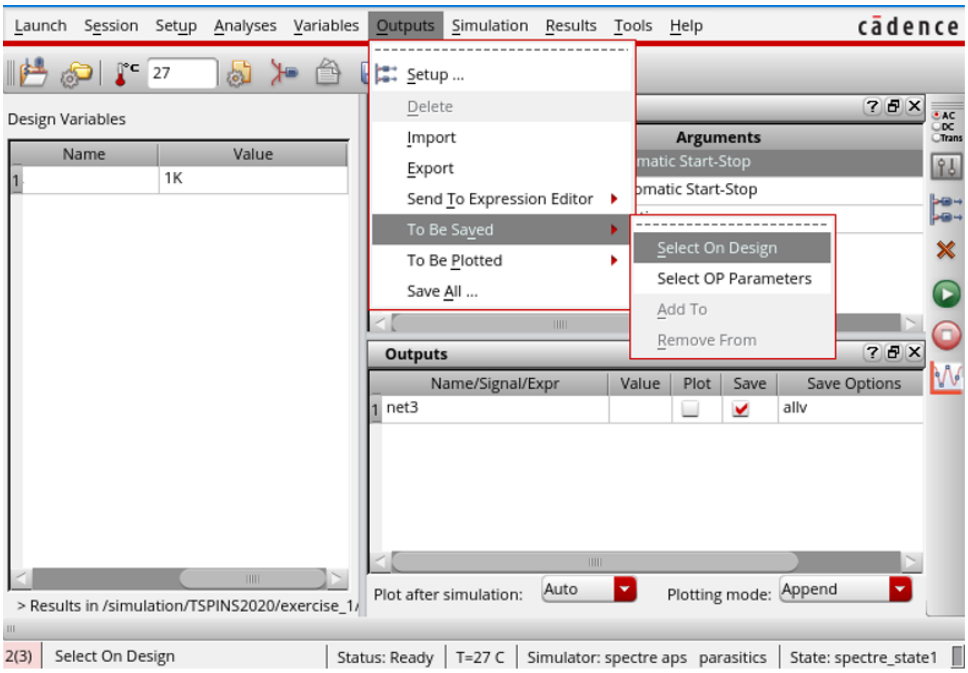


Fig. 3 Save DC Operating point

7. Select "Stimulation"→"Netlist and Run". After the simulation is completed, in the ADE L window under the "Output" dialog box (lower right box), tick the Plot option, and click on "plot outputs" icon (circled in red) as illustrated in Fig.4. The simulation results will pop up on the main screen. Capture the screen and report what is the value of R_{REF}.

   Press the following shortcut keys in the simulation result window help you to view details of the waveform. "V" for the vertical scale line, "H" for the horizontal scale line, "M" for marking the parameters on the waveform, "A" and "B" to measure the distance.

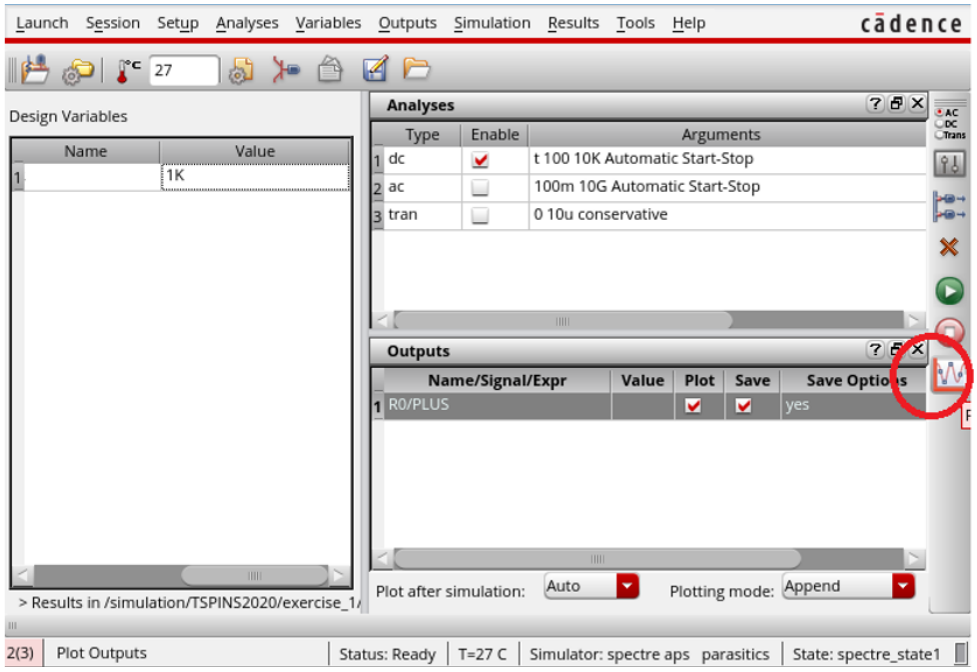


Fig.4 The view method of simulation results

8. To ensure that the transistors are working in saturation region, you need to check the "DC Operating Points" of all transistors. Select "Results"→"Print" →"DC Operating Points", as shown in the Fig. 5. Then go back to the schematic window and use your mouse to click on the transistor, the DC operating points will be printed next to each device. The result of "DC Operating Points" of the transistor will pop up in a window. Based on DC operating points, determine if all transistors are in saturation region.

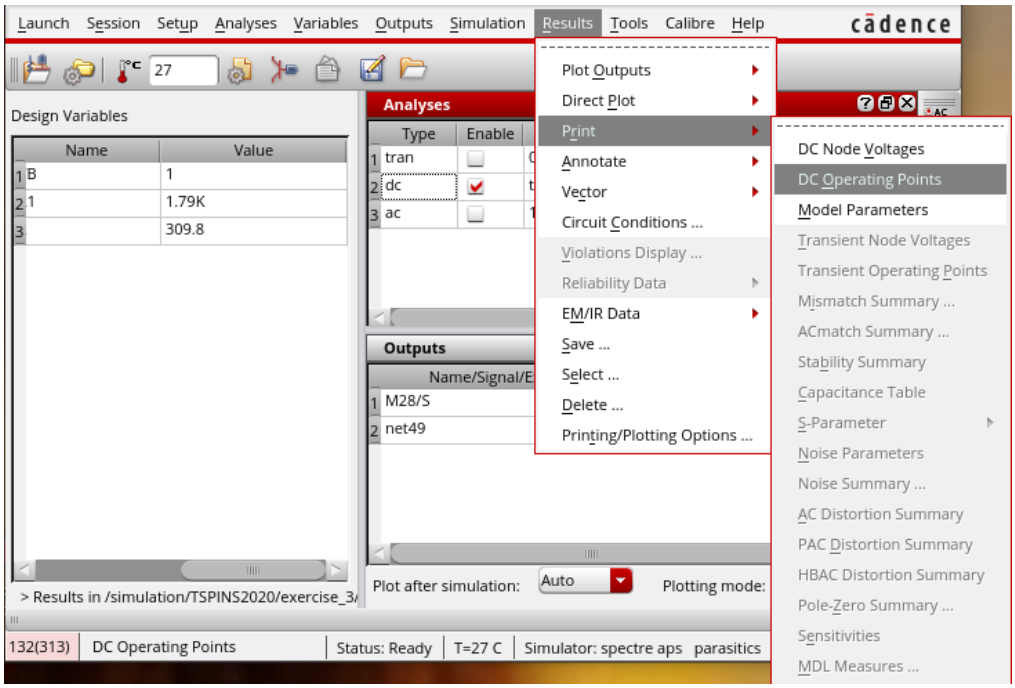


Fig.5 Print DC Operating Points

9. To obtain the gain of a circuit, you need an AC signal source for the amplifier. Press the shortcut "i" to insert a device, a window pops up. Select "analogLib"→ "vsin" under Cell, and you should enter the DC voltage value under "DC voltage" option and the "AC magnitude" option to complete the setting as illustrated in Fig.6.

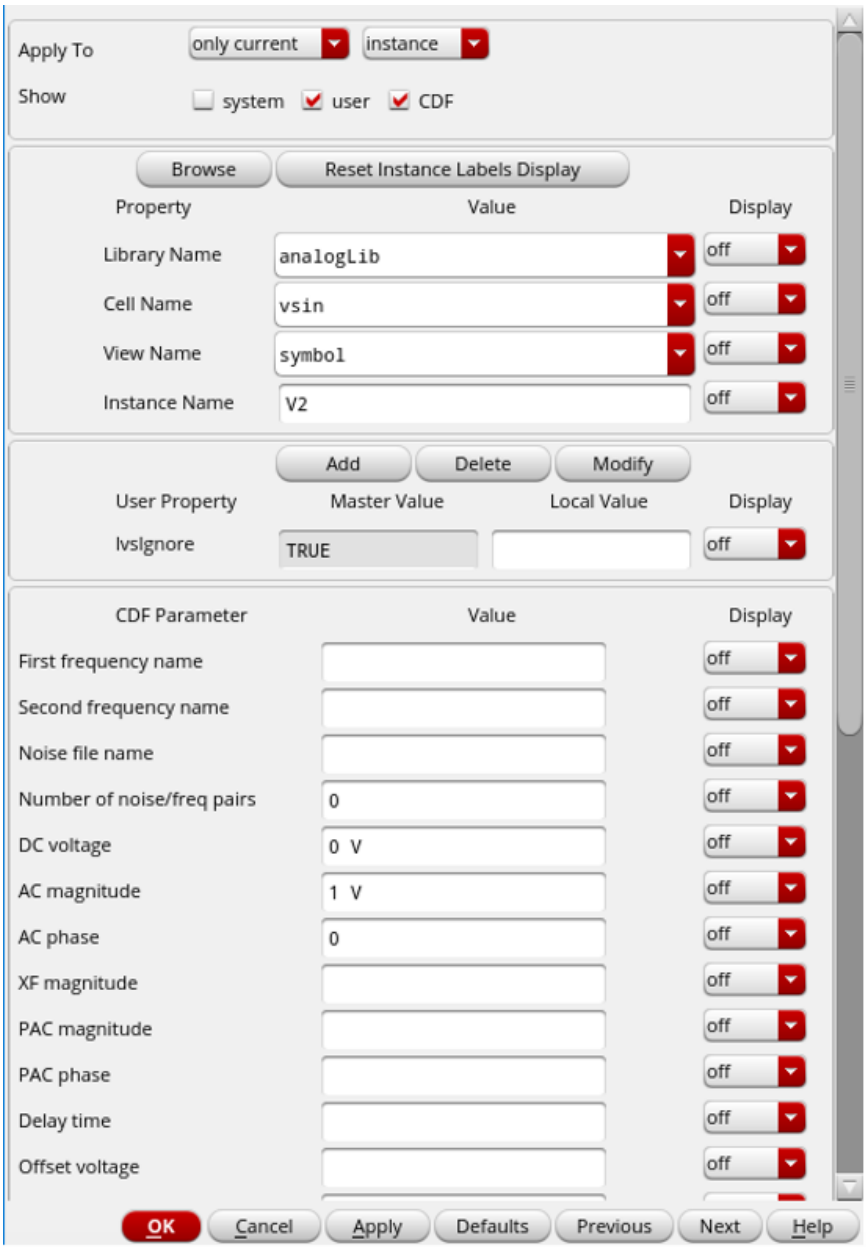


Fig.6 AC small signal excitation setting

10. Select "Analyses"→"Choose" command in the ADE window. In the pop-up dialog box pops, select "ac", "Design Variable" under the Sweep Variable (then click Select Design Variable) to complete the setting as shown in Fig.7. Note you need to set a working frequency, enter 1M under "At Frequency" option.

Fig.7 AC simulation Configuration

11. Set R1 as a variable if you need to design R_1 for a given gain. Then run simulation by selecting "Stimulation"→"Netlist and Run". After the simulation is completed, select "Results"→ "Direct Plot"→"AC Magnitude", then click the output as shown in Fig.8. The simulation result will be printed. Capture the screen, and report what is the value of R_1 when the overall gain is 6.

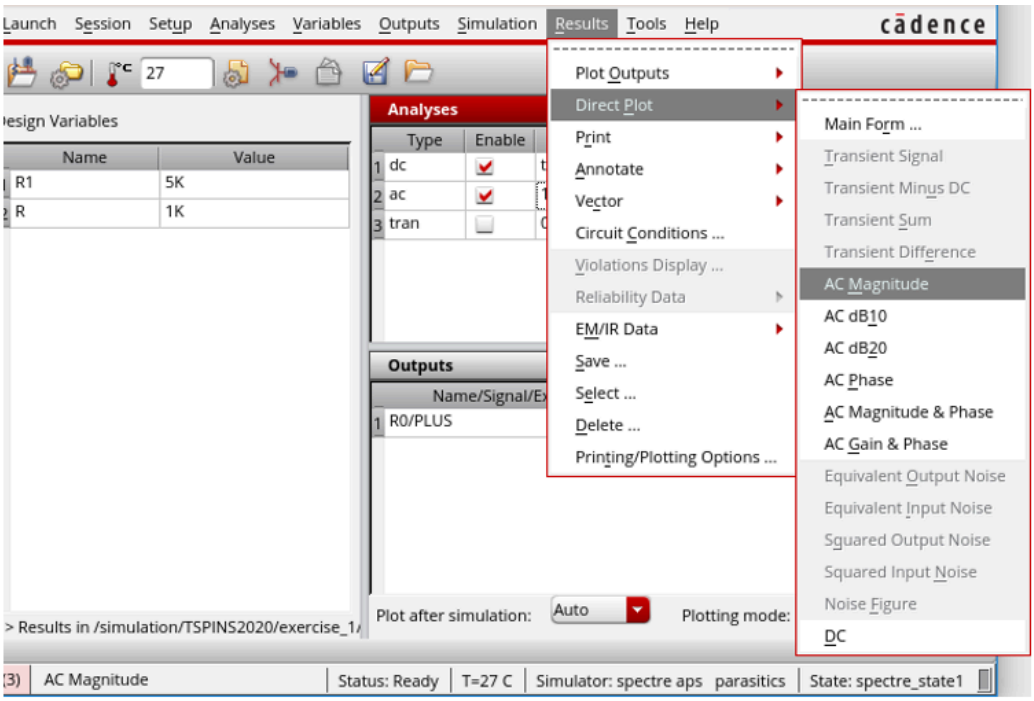


Fig.8 AC simulation result setting

12. Enter the value of R_1 you get, and run the simulation again to verify the correct gain. This can be done by opening the "AC Analysis", tick "Frequency" in the option bar "Sweep Variable", and enter the start-stop frequency range, as shown in Fig.9, and repeat the simulation.

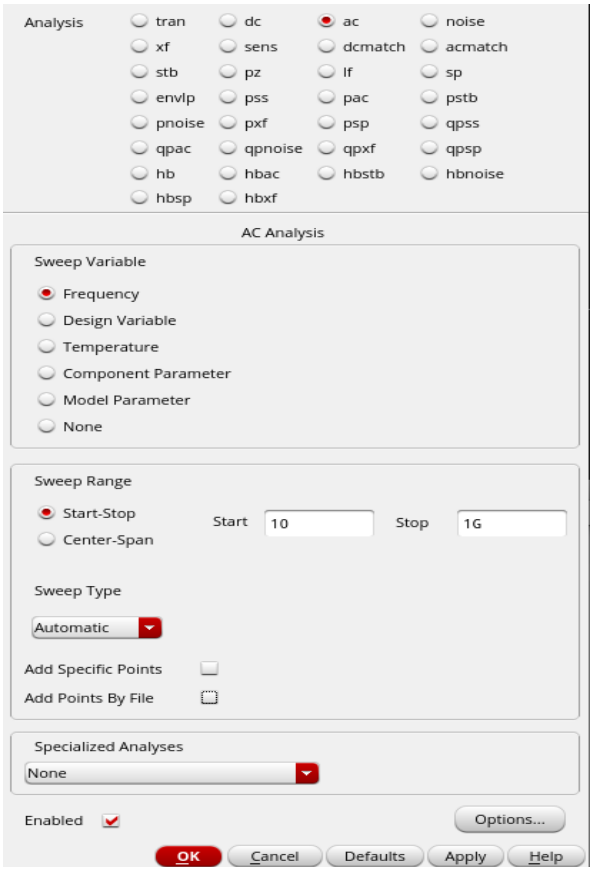


Fig.9 AC simulation Configuration

Report what you get, is the gain meeting the design goal?

13. To observe the output waveform, set values for a sinusoidal signal, e.g. input signal with frequency of 1MHz and peak-to-peak amplitude of 100mV as shown in Fig.10.

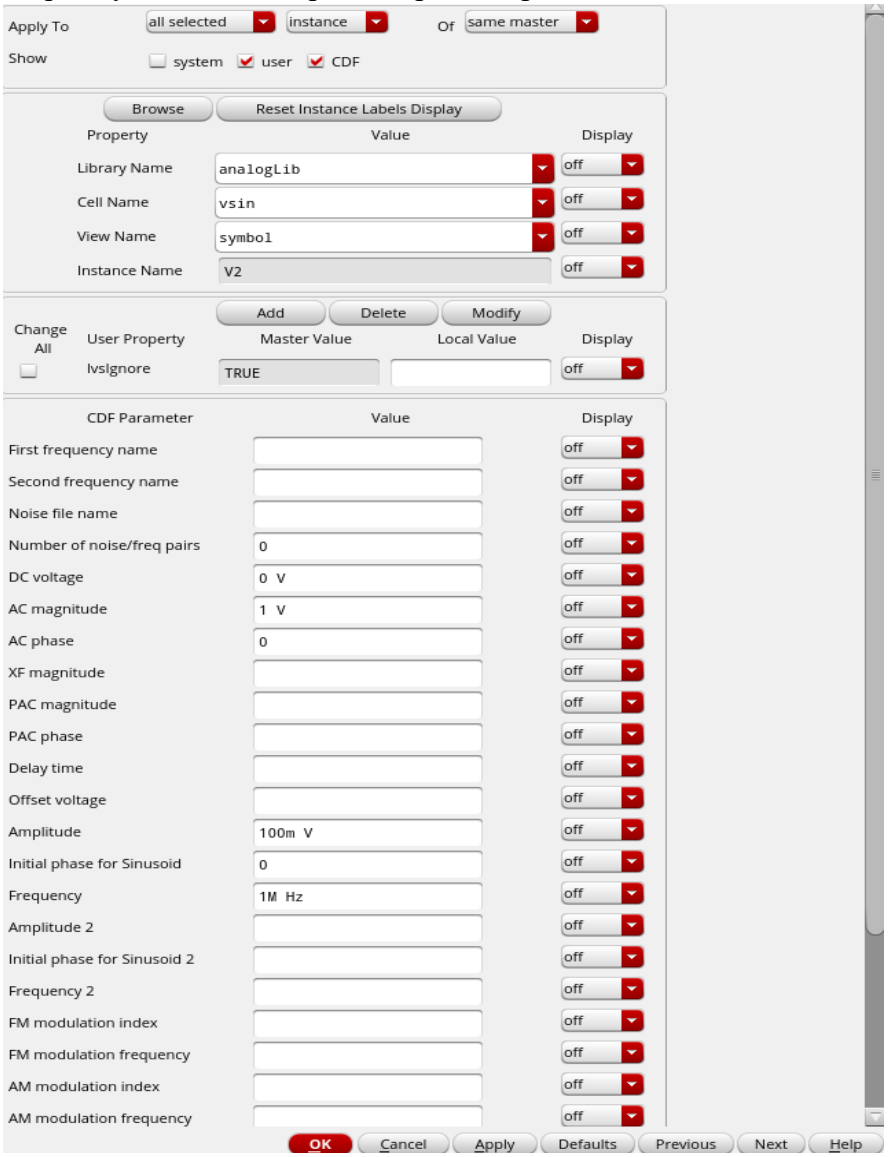


Fig.10 The Transient signal setting

14. Select the "Analyses"→ "Choose"→ "tran". Enter the Simulation Time "10u" in the "Stop Time", select "Conservative" under the "Accuracy Defaults", then click the "OK" to complete the setting as shown in Fig.11.

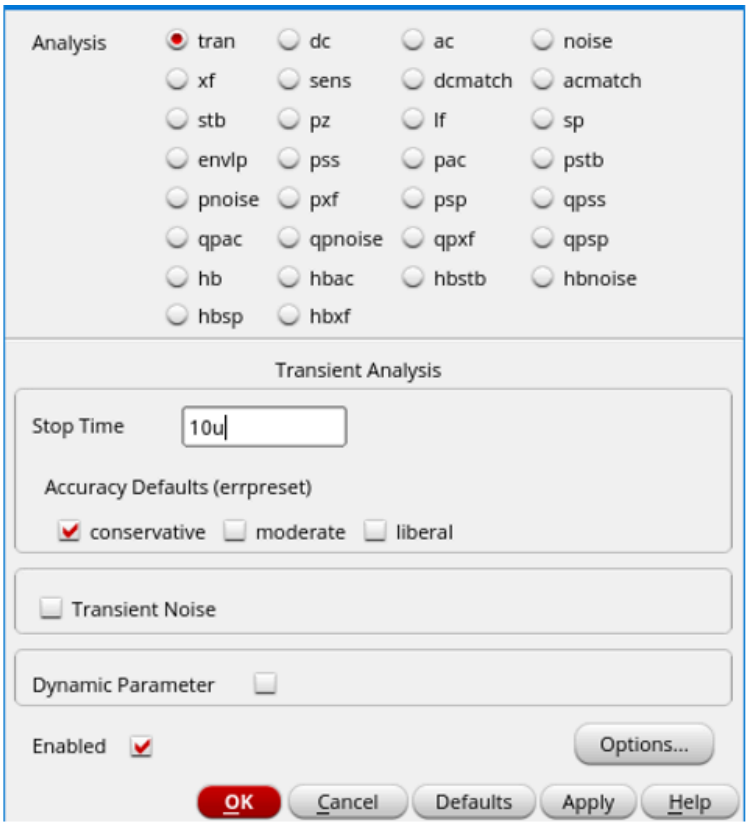


Fig.11 Tran simulation Configuration

15. Select the "Outputs"→"To be saved"→"Select On Design " and click on the output port. Select "Simulation"→"Netlist and Run" to perform the simulation.

16. Select "Results"→ "Direct Plot"→ "Transient Signal", as shown in Fig.12.

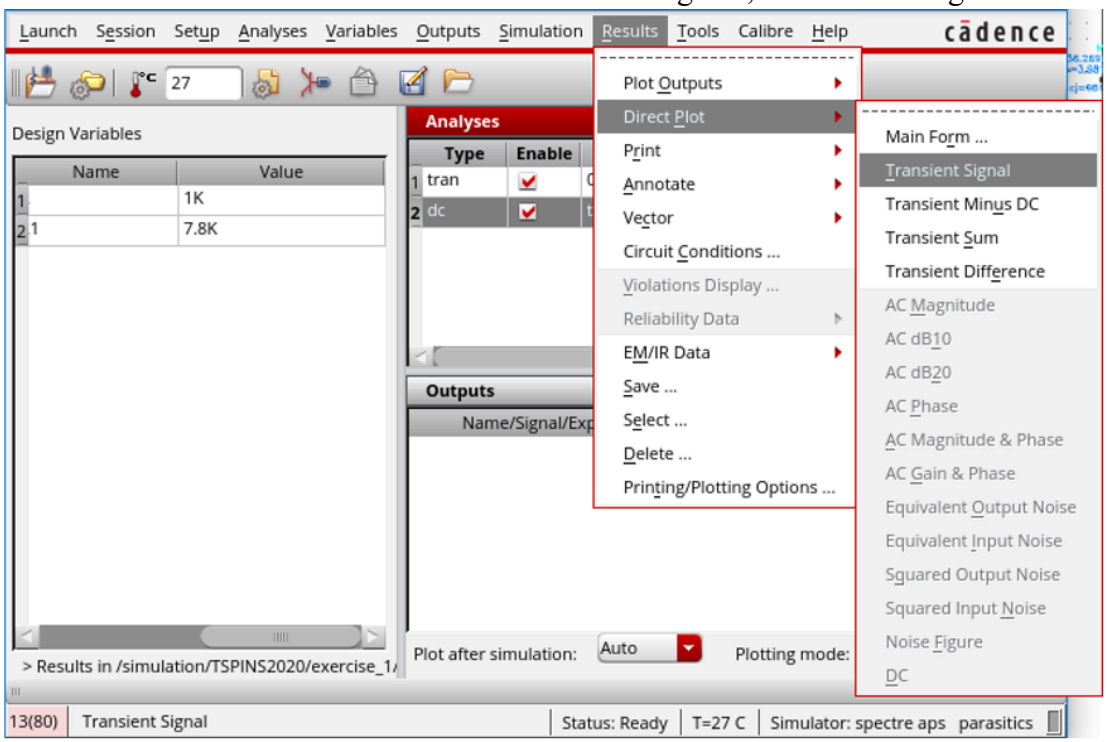


Fig.12 TRAN simulation result setting

What is your observation from the output waveform? Suggest a fix, then run the simulation again until the output waveform is correct. Report the process including the modified circuit, device sizes, DC operation points, and output waveform for modified circuits.

Instructions for Lab Exercise 2

1. Make sure you add a supply voltage source of 2V during schematic creation. You can use "vdc" device to provide DC supply voltage. You also need an excitation signal to simulate the gain of the amplifier (vsin), set AC magnitude as 625mV.
2. Select the "Analyses"→"Choose" command in the ADE window, a dialog box pops up. Select "dc"→"Save DC Operating Point " (and click "OK" Button to complete the setup.
3. Select the "Analyses"→"Choose"→"ac", at the "Start" and "Stop" columns， you should set the Start =1 and the Stop=1G (indicating that the frequency of scanning ranges from 1Hz to 1GHz). Then select the default "Automatic" in the "Sweep Type". To determine R_s and R_B for a f_U of 40MHz, set R_S as a Design Variable R and R_B as a variable of 100*R, set "At Frequency" to 40MHz.
4. Select the "Outputs"→"To be saved"→"Select On Design " and click on the output port.
5. Select "Simulation"→"Netlist and Run". After the simulation is completed, select "Results" →"Annotate" →"DC Operating Point"(DC Node Voltages), by this way, you should find the DC operation point under the circuit.
6. By checking the DC operating points of the circuit, you should confirm that the transistors are working in the saturated region. Select "Results"→ "Direct Plot"→ "Main Form"→"dB20" and click the line of "VOUT" of the circuit, as shown in Fig. 13. Use "Esc" key to terminate the selection as shown below. The simulation results will pop up on the main screen. Capture the screen and report the value of R.

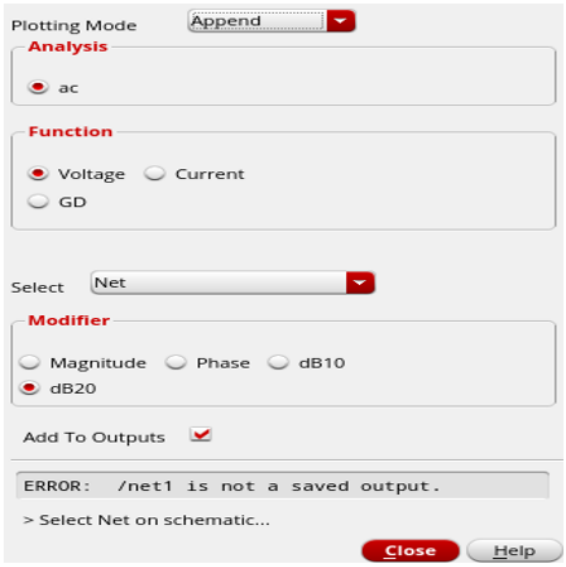


Fig.13 Direct Plot Form

7. Verify that selected R_s and R_B lead to a f_U of 40MHz. Show the waveform in your report.
8. To design C_L such that the f_L is 50Hz, you can set C_L is a variable and run AC analysis at 50Hz. What is the value of C_L? Report the process on how to determent C_L and verify that the selected C_L meets the design goal.