EECS3611 Operational Amplifier Design Project

The objective of this project is to design and simulate an operational amplifier. You will use TSMC180nm CMOS process for the project. The design specifications are given in the table below. This is an individual project.

Table I Design specifications

Parameter	Value
V_{DD} (DC power supply)	1.8V
I_P (total DC current drawn from power supply)	≤5mA
C_L (load capacitor)	≤2pF
A_v (voltage gain)	≥1000V/V (60dB)
GBW (unit gain bandwidth)	≥10MHz
SR (slew rate)	≥10V/μs
PM (phase margin)	≥60°
ICMR (input common mode range)	0.8 to 1.4V
Output swing	0.4 to 1.5V

Tasks

1. Design and simulate an op-amp using MOS devices, which meets the specifications given in Table I. You are not allowed to use any ideal current source for biasing. You can use resistors and capacitors for biasing and compensation. The maximum allowed W/L ratio for any MOS device in the amplifier is 1000.

2. Do analytical calculation and verify them in simulation.

3. Submit a report before the deadline.

Project Report

Your project report should include the followings:

1. A cover page including title, name, student number and date.

2. An introduction

3. Description of your design including (a) overview of your circuit and how the different parts function (b) hand calculation for your design: how you choose the W/L ratio for the transistors, how you know the specifications are met without simulation

4. Simulation results of your design including (a) testbench setup (b) appropriate plots to show that the specifications are met (hint: you need to perform DC, AC and transient simulations for different specifications. For slew rate, using a step of 0.5V input pulse for simulation)

5. Discussion and conclusion including (a) a comparison table for the transistor sizes obtained from hand calculation and those obtained after verification by simulation (b) a comparison table for the given specifications and your simulation results (c) discussion on the discrepancies in (a) and (b)

Parameters for nmos2v and pmos2v in TSMC180nm technology

In this project, you may consider using the devices nmos2v and pmos2v. Their parameters can be found in */CMC/kits/cmosp18.6.13a_ic6/models/spectre/cmn018_assp_v1d3.scs* and the most commonly used ones are concluded here:

For nmos2v:

$V_{th0,n}$ = 0.4395 V // threshold voltage

$t_{ox,n}$ = 3.981 nm // electrical gate oxide thickness

$\mu_{0,n}$ = 0.0305 $m^2/(V \cdot s)$ // base mobility

λ_n = 0.719 // channel length modulation factor

For pmos2v:

$V_{th0,p}$ = -0.459 V // threshold voltage

$t_{ox,p}$ = 4.06 nm // electrical gate oxide thickness

$\mu_{0,p}$ = 0.0139 $m^2/(V \cdot s)$ // base mobility

λ_p = 0.491 // channel length modulation factor

and

ε_{ox}=3.9 x 8.85 x 10^{-12} F/m // absolute permittivity of SiO_2

$C_{ox,n} = \varepsilon_{ox}/t_{ox,n}$

$C_{ox,p} = \varepsilon_{ox}/t_{ox,p}$