

Tutorial

Running ModelSim From Within Quartus



EECS 3216, Digital Systems Engineering
Modelling, Implementation and Validation

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1 MODELSIM FROM WITHIN QUARTUS

This tutorial describes, how to run a ModelSim simulation (RTL) from within the Quartus SW IDE.

Follow the steps described here for running ModelSim from within the Quartus Software.

It is **assumed** that you have already Installed Quartus 20.1 Lite, the Max10 Device files and ModelSim simulator, as described in the '*Tutorial_QuatusInstallAndVerify*' document, which describes steps to install the SW and test your setup.

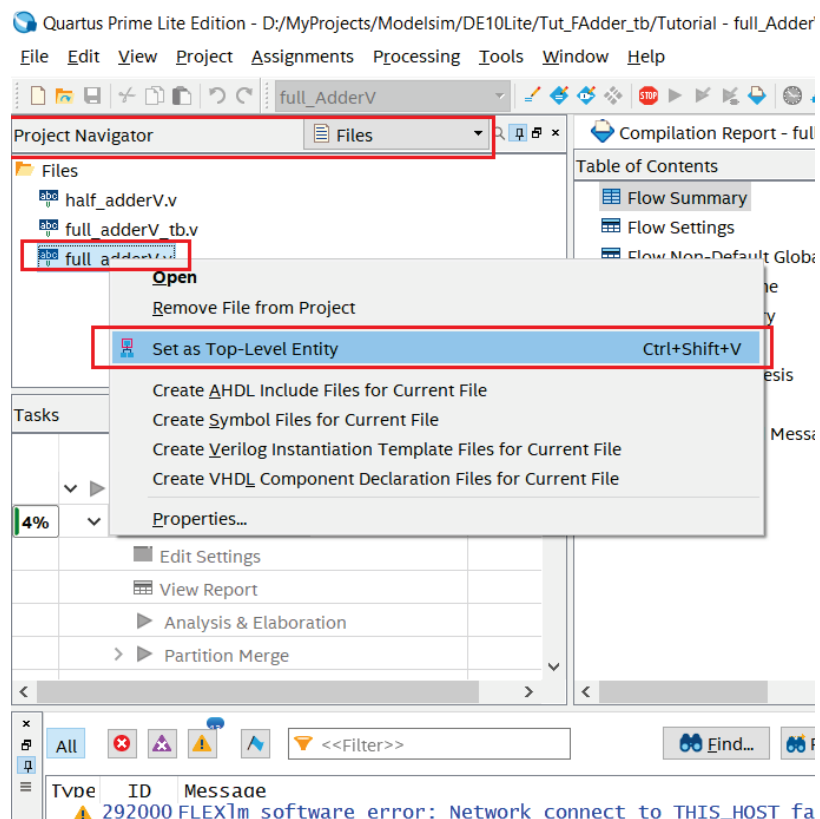
1.1 SETUP WITHIN QUARTUS

1. Download and save the following three Verilog files provided on the eClass website.
The files contain design of a Full Adder and a Test bench.

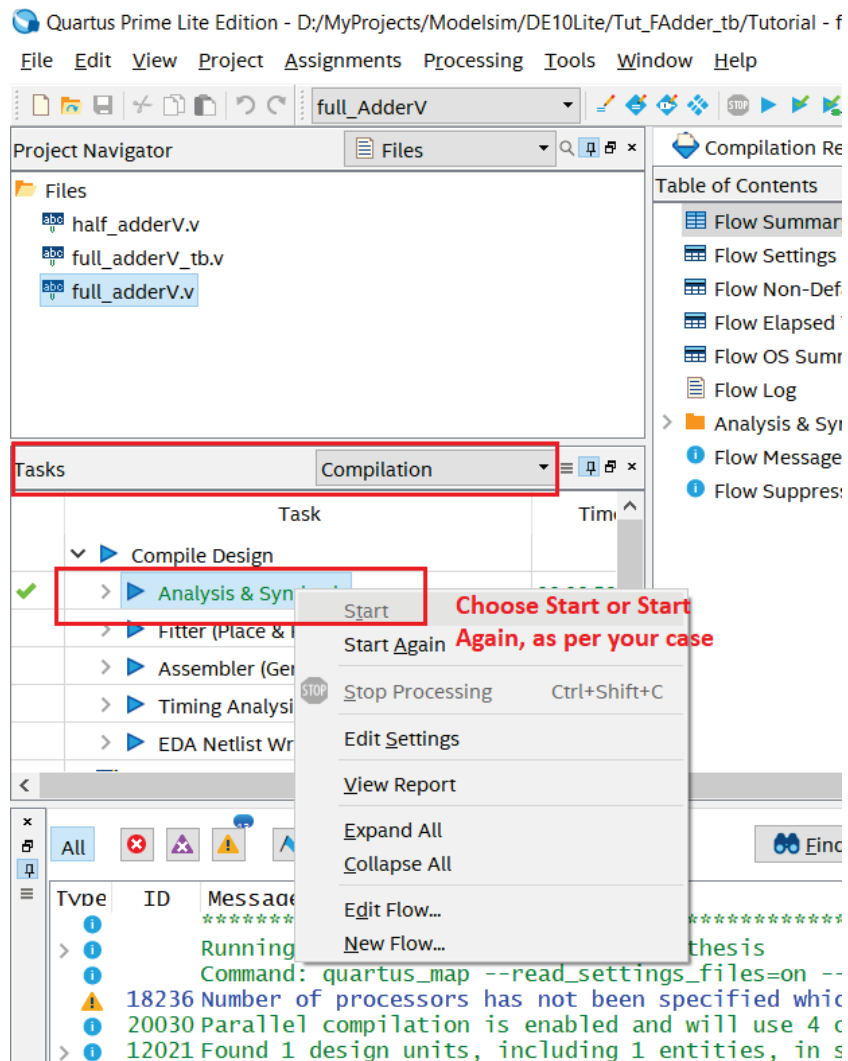
half_adderV.v
full_adderV.v
full_adderV_tb.v

This is a simple testbench.

2. Now follow the instructions in the '*Tutorial_QuatusInstallAndVerify*' document, to create a project using these files. Use a suitable *project directory*, *project name* however enter **full_adderV** as your top_level module.
3. Add three provided files in the project you created, following the steps in '*Tutorial_QuatusInstallAndVerify*' document.
4. Make sure that **full_adderV** is indeed the top level, by right clicking on the file name and selecting 'set as top level entity' as shown below.



5. Run the 'Analysis and Synthesis' which is a step within the Compile Design process.

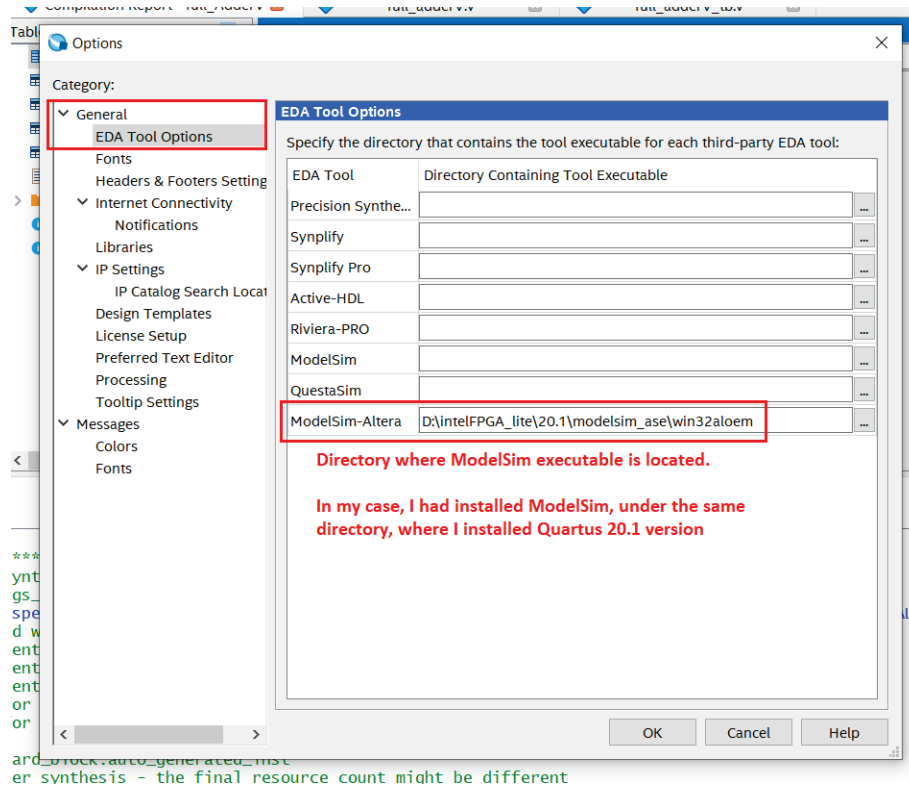


Pay attention to any code or syntax related Error messages, before proceeding to RTL Simulation, for you will likely get them in ModelSim too.

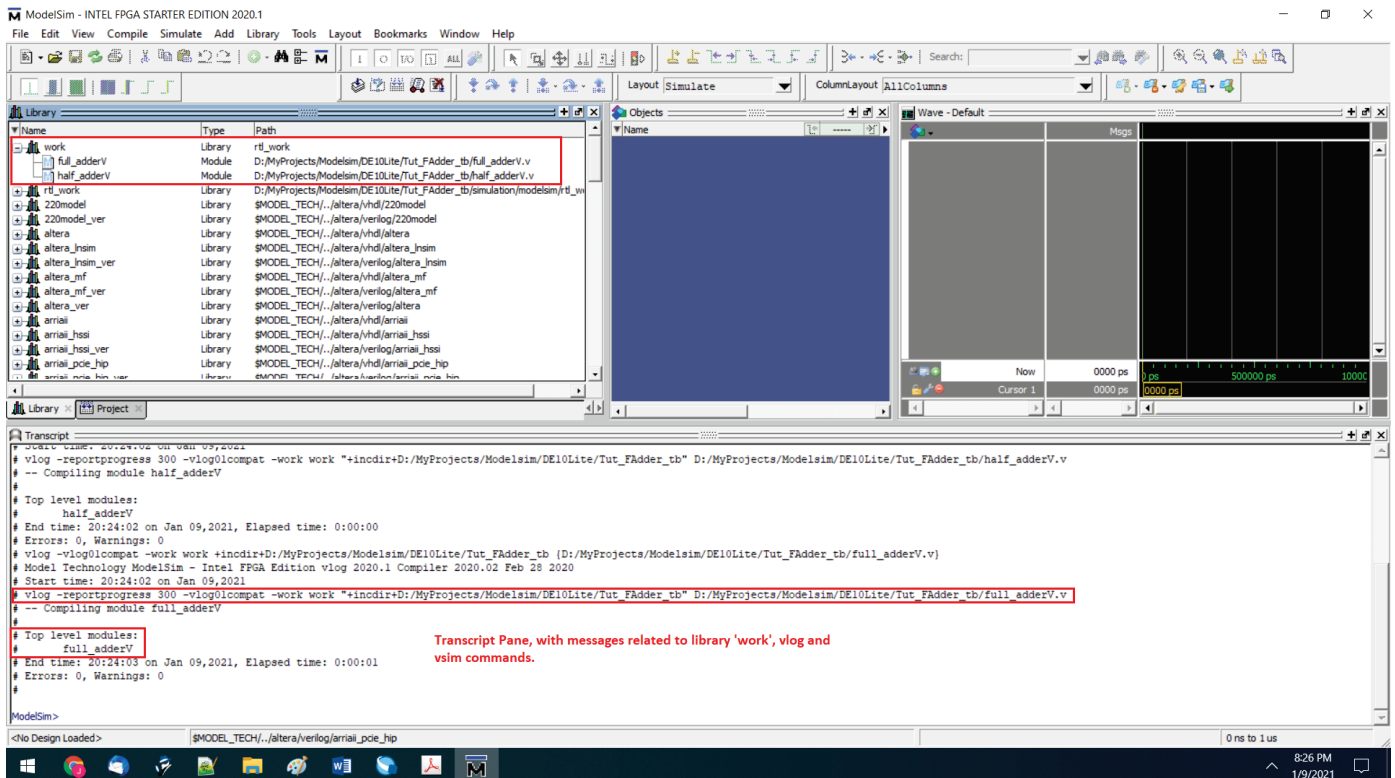
1.2 START RTL SIMULATION

After your design compiles satisfactorily, you are ready to start ModelSim simulator. If encountered code or syntax related Error messages, try fixing them, before proceeding to RTL Simulation.

However before ModelSim can be run, it is required to specify the path, where the ModelSim executable is located. Specify it by going the **menu Tools -> Options** and the Selecting 'EDA Tool options' under the General settings and specify your specific path, where the executable is located.



After having specified the path, run ModelSim by selecting menu -> **Run Simulation Tool -> RTL Simulation**. If you followed all the steps correctly, including steps in 'Tutorial_QuartusInstallAndVerify', ModelSim would now start and you would see the following screen.



You would see both 'full_adderV' and 'half_adderV' in the 'work' library.

1.3 ADD TESTBENCH OR OTHER FILES

To also add the testbench, 'full_adderV_tb' go menu **Compile -> Compile...** which opens the 'Compile Source Files' window.

- By default it opens within the 'modelsim' folder of your Quartus project.
- Browse to the directory, i.e. your parent Quartus project directory, which contains your Design and the Testbench files.
- Since the two design files are already in the ModelSim library, just select the testbench file and click on Compile.
- After the compile operation, click Done, to close the window.

ModelSim - INTEL FPGA STARTER EDITION 2020.1

File Edit View Compile Simulate Add Library Tools Layout Bookmarks Window Help

Library

Name	Type	Path
work	Library	rtl_work
full_adderV	Module	D:/MyProjects/Modelsim/DE10Lite/Tut_FAdder_tb/full_adderV.v
half_adderV	Module	D:/MyProjects/Modelsim/DE10Lite/Tut_FAdder_tb/half_adderV.v
rtl_work	Library	D:/MyProjects/Modelsim/DE10Lite/Tut_FAdder_tb/simulation/modelsim/rtl_w

Compile Source Files

2. Make sure you see Library as 'work'

1. Go to the directory with your Source files.

Library: work

Look in: Tut_FAdder_tb

Name	Date modified	Type
db	1/9/2021 8:23 PM	File f
incremental_db	1/9/2021 2:59 PM	File f
output_files	1/9/2021 8:21 PM	File f
simulation	1/9/2021 7:30 PM	File f
full_adderV	1/9/2021 2:58 PM	V File
full_adderV_tb	1/9/2021 3:00 PM	V File
half_adderV	1/9/2021 2:34 PM	V File

3. Select the file or files, you want to Compile.
In our case, only 'full_adderV_tb' is fine

4. Click Compile

File name: full_adderV_tb

Files of type: HDL Files (*.v;*.vl;*.vhd;*.vhdl;*.vho;*.hdl;*.vo;*)

5. After compile is done click, Done

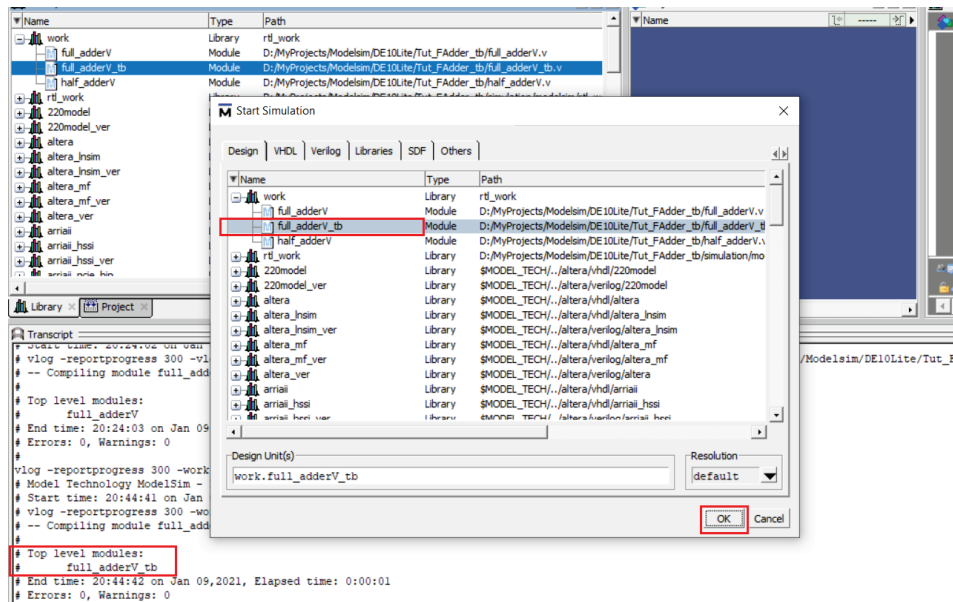
Transcript

```
Start time: 20:24:03 on Jan 09, 2021, Elapsed time: 0:00:01
# vlog -reportprog
# -- Compiling mod
#
# Top level module
#   half_adder
# End time: 20:24:03 on Jan 09, 2021, Elapsed time: 0:00:01
# Errors: 0, Warni
# vlog -vlog0lcomp
# Model Technology
# Start time: 20:24:03 on Jan 09, 2021, Elapsed time: 0:00:01
# vlog -reportprog
# -- Compiling mod
#
# Top level module
#   full_adderV
# End time: 20:24:03 on Jan 09, 2021, Elapsed time: 0:00:01
# Errors: 0, Warnings: 0
#
```

You will now see that 'full_adderV_tb' has also been compiled and added to the 'work' library and it has now become the Top level module.

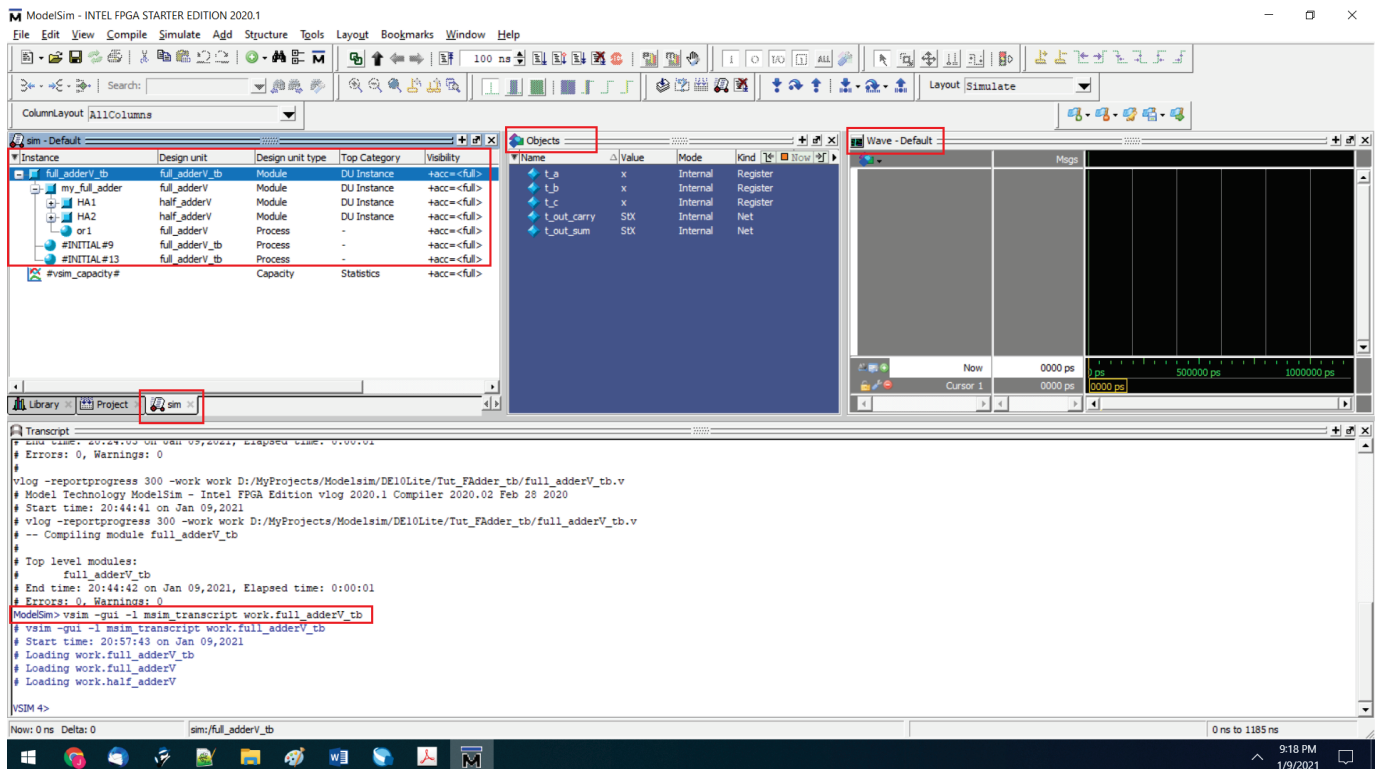
1.4 START SIMULATION

Now you are ready to start simulating. Do menu -> **Simulate** -> **Start Simulation**. In the window which opens, select 'full_adderV_tb' and click OK, as shown below.



This runs the 'vsim' command, which starts the Simulator. You will now see

- A new 'Sim' tab, which shows your Top level module and the lower instances below it.
- An 'objects' window, which shows the 'Signals' as per the selected Instance, in the Sim tab.
- A 'Wave' window, to which the Signals can be added and on running the Simulation, results are seen as a waveform, on those signals.



1.5 ADD SIGNALS

We now add the signals to the Waveform window, before running the Simulation, as shown below.

To add the signals to the Wave window do

- Select the appropriate instance, in the 'Sim' tab
- You will now see the signals of this instance, within the 'Objects' window.
- Select the signals, you want displayed and right-click you mouse, and then select 'Add Wave' to add in the Wave window.

As you add the signals, the Transcript Pane will display corresponding messages.

The screenshot displays the ModelSim - INTEL FPGA STARTER EDITION 2020.1 interface. The main window is divided into several panes:

- Instance:** A tree view showing the design hierarchy. The instance 'my_full_adder' is selected. A red text overlay states: "Instance 'my_full_adder' is selected. Its name given to the module 'full_adderV' in the testbench."
- Objects:** A table listing signals under 'my_full_adder'. A context menu is open over the selected signals, with 'Add Wave' highlighted. The table has columns: Name, Value, Mode, Kind, and a 'Show' button.
- Wave - Default:** A waveform window showing a time axis from 0 to 100,000 ps. A cursor is positioned at 0 ps. A red text overlay above the waveform reads: "Previously added signals from the testbench".
- Transcript:** A log window showing simulation progress and commands. The transcript includes:

```
ModelSim> vsim -gui -l msim_transcript work.full_adderV_tb
# Start time: 20:57:43 on Jan 09, 2021
# Loading work.full_adderV_tb
# Loading work.full_adderV
# Loading work.half_adderV
add wave -position insertpoint \
sim:/full_adderV_tb/t_a \
sim:/full_adderV_tb/t_b \
sim:/full_adderV_tb/t_c \
sim:/full_adderV_tb/t_out_carry \
sim:/full_adderV_tb/t_out_sum \
NSIM 5>
```

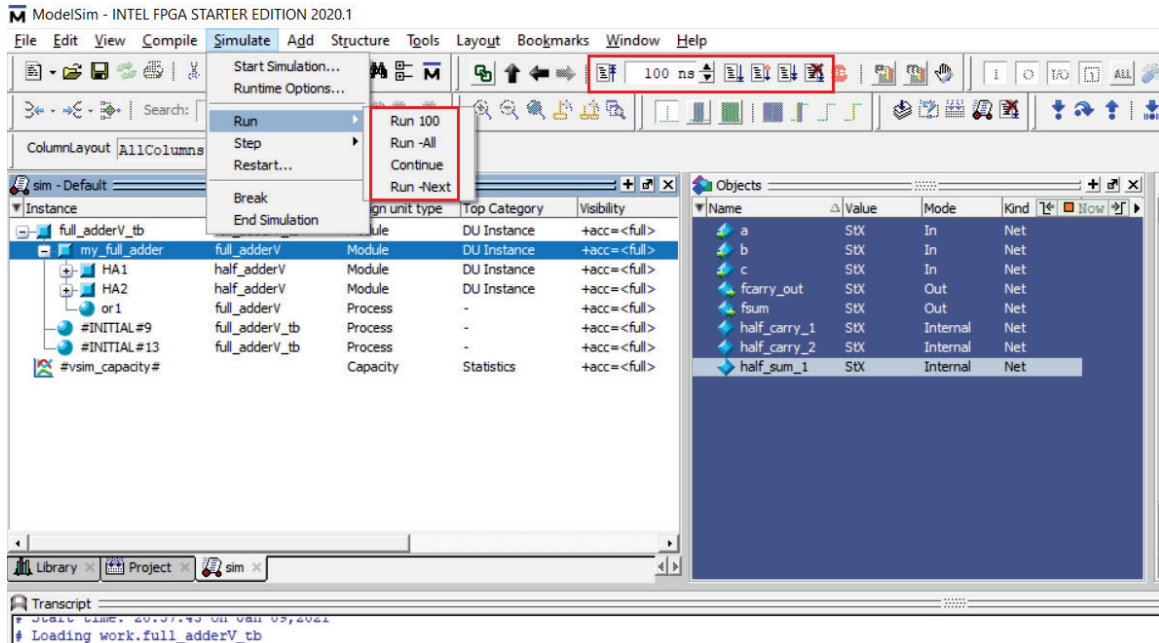
1.6 RUN SIMULATION

To run the simulation, few options are available.

- **Run 100ns**, will run the simulation for 100ns, or as per time specified by you.
- **Run -All** will continue running the simulation, till a *Breakpoint* is hit or a statement like *\$stop* is hit.

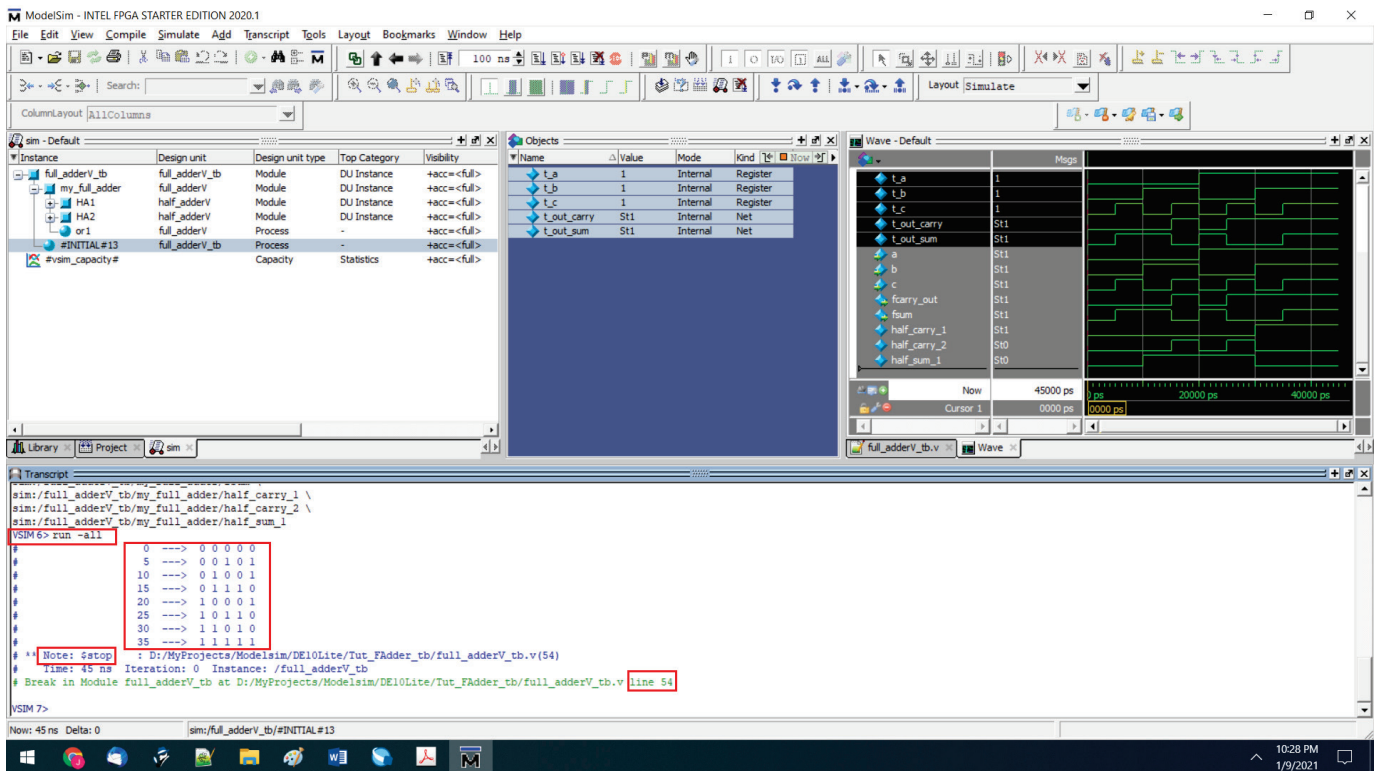
You can stop a simulation, by selecting the 'Break' command.

The commands can be run from the **menu Simulate -> Run ->** or from the **Icons** shown, **or by typing** in the Transcript pane.



Since in our testbench there is a *\$stop* statement, at the end, just type **run -all** (lowercase) in the *Transcript* pane.

In our case, you will see that Transcript pane shows the signals, anytime one of them changes, due to the *\$monitor* command. Further, the Wave window shows the top level, testbench signals as well signals of the instance, 'my_full_Adder'



You can try additional things like adding more signals to wave window, from other instances in your design, e.g. from the Half Adder, and **restart** your simulation and run it again.

To end your simulation, do **menu Simulate -> End Simulation**

You exit ModelSim, by doing **menu File -> Quit** This closes ModelSim and takes you back to the Quartus SW.

This concludes the tutorial.

1.7 ADDITIONAL INFORMATION

Refer to the online resources on ModelSim, including the **ModelSim User Manual** and **Mentor ModelSim Tutorial** which provide lot more detail about additional features of this tool, particularly in using this simulator in a Standalone mode, independent of Quartus software.