Tutorial

# Quartus Install and Verify Setup



# EECS 3216, Digital Systems Engineering Modelling, Implementation and Validation

Winter 2021

By Jaspal Singh, Engineering Technologist, Lassonde School of Engineering. EECS York University, Toronto.

# **1** QUARTUS SW INSTALL AND TESTING INSTRUCTIONS

# 1.1 FOR THE WINDOWS SYSTEMS

1. Link for Download (You will have to register, before downloading)

https://fpgasoftware.intel.com/

Currently go for version **20.1 (Lite)** version which is free. Download file size is around 2GB, while the total install size (Quartus, ModelSim, Device files) is around 14 GBytes and it takes <u>about an hour</u>, for the installation!

You may have to disable your virus protection, while downloading and installing. Due to download sizes, it might be better to download **Individual Files**, instead of the combined files.

In that case, download the following files individually and install them sequentially.

- Quartus Prime Lite Edition (including the NIOS EDS)
  - For using the DE10-Lite board, you will also need to install the..
- Max 10 FPGA device support file. (if you download this file, at the time of Quartus install, this driver would get installed automatically)
   \*\*Note\*\*, if you have **already** downloaded the device files, *Quartus at the time of it's Install* will give you the option to install the downloaded Device files also, the same time.
- ModelSim Intel FPGA Edition
   \*\*Note\*\*, when installing ModelSim, point it to the *same directory*, where you installed Quartus, e.g. C:\IntelFpga\_lite\20.1 or as per your own case.

For your reference, also download the '*Intel Quartus Prime software, User Guide*' This document will help you get acquainted with the software's IDE.

Use one of the following links:

https://www.intel.com/content/www/us/en/programmable/products/design-software/fpga-design/quartus-prime/user-guides.html

https://tinyurl.com/y7xaw5u4

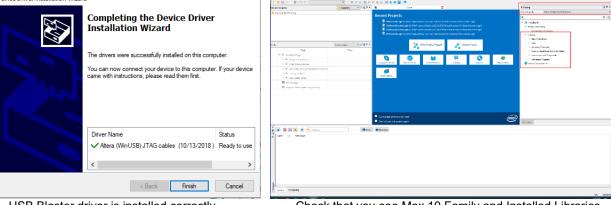
#### 1.1.1 INSTALLING QUARTUS AND MAX 10 DEVICE FILES

	10/10/0000 7.00 014				
!947 Lab	Installing Quartus Prime Lite Edition (Free) 20.1.0.711 —	D X	m 47	Installing Quartus Prime Lite Edition (Free) 20.1.0.711	- 🗆 X
4 r Ne ig	Installation directory	(intel)	ap Ac	Select Components	(intel)
)eve	Specify the directory where Quartus Prime Lite Edition (Free) 20.1.0.711 will be installed			Select the components you want to install	
gn_(	Installation directory D:\intelFPGA_lite\20.1			🗄 🗹 Quartus Prime Lite Edition (Free)	You can add additional device support to an existing Ouartus Prime software installation without having to
nula				Quartus Prime (Includes Nios II EDS) (9313MB)	reinstall the entire software package. Use the Install Devices command on the Tools menu in the Quartus Prime
iseL			sit. Je	🗹 MAX 10 PPGA (360.3MB)	software to get started. Select a component for more information
ng					
fun					
IAg			In		
v3			Ac		
			3		
CAL					
io 2			1		
Bilo			12		
Mai			lo		
	InstallBuilder		ai <sup>II</sup>	installBuilder	
aSac	< Back Next >	Cancel	an	hal eeiai 5/8/	< Back Next > Cancel 2020 11:07 AM MPEG File

Specify the Install Directory

#### If already downloaded Max10 Device file, check it off

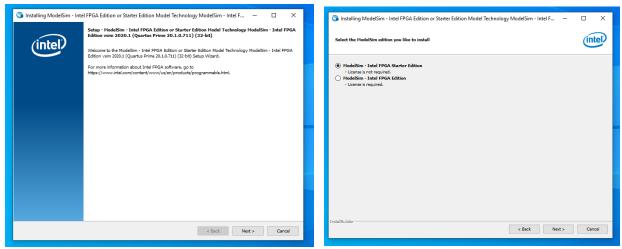
mr 47	S Installing Quartus Prime Lite Edition (Free) 20.1.0.711	- 🗆 ×	X S Installing Quartus Prime Lite Edition (Free) 20.1.0.711 —	×
əb Ne	Ready to Install	(intel)	/intel2	
ve L( ula EL	Summary: Installation directory: D:\intelPFGA_lte\20.1 Required disk space: 5676 MB Available disk space: 329451 MB		Setup has finished installing Quarture Prime Lite Edition (Free) 20.1.0.711.  Setup has finished installation  Create shortcuts on Desktop  Launch Quartus Prime Lite Edition  Provide your feedback	
یں 4g 3 4L 20				
an	Installouider Signature Signat	xt > Cancel	d <back cana<="" prish="" th=""><th>el</th></back>	el
6	Device Driver Installation Wizard	- b 100 74		- 5 X
	Completing the Device Driver Installation Wizard	Fea.ect Variantee		X
d	The drivers were successfully installed on this computer. You can now connect your device to this computer. If you came with instructions, please read them first.	r device	Vis         Vis <th></th>	



USB Blaster driver is installed correctly.

Check that you see Max 10 Family and Installed Libraries

## 1.1.2 INSTALLING MODELSIM



Select the free 'Starter' Edition

🕥 Installing ModelSim - Intel FPGA Edition or Starter Edition Model Technology ModelSim - Intel F – 🛛 🗙	🕥 Installing ModelSim - Intel FPGA Edition or Starter Edition Model Technology ModelSim - Intel F — 🛛 🛛 🗙
License Agreement	Installation Directory
You can view the full icanse agreement at the link below. You must accept the terms of the agreement before continuing with the installation. http://ficaachuare.intei.com/eula/	Specify the directory where ModeSim - Intel FPGA Starter Edition 20.1.8.711 will be installed Installation Directory DivinalPDGA_lite120.1
88. quickserver 1.4.7 (LGPL v.2.1 License)         89. syningworker 3 (MPL v. 1.1 and LGPL v. 2.1 Licenses)         90. symphony 5.4.5 (Eclipse Public License v. 1.0)         91. syntemic 2.2.0 (Systemic Open Source License v. 3.3)         92. velocity 1.4 (Apache v. 2.0 License)         93. wraph 0.2 (Apache v. 2.0 License)         94. xalian 1.2.2 (Apache v. 2.0 License)         95. xerrese 2.3.2 (Apache v. 2.0 License)         96. serrese 2.12.0 (Apache v. 2.0 License)         97. xmibeans 2.2.0 (Apache v. 1.1 License)         97. xmibeans 2.2.0 (Apache v. 2.0 License)         © I accept the sgreement	
Installbulder Cancel	InstalBuilder Cancel

Use same Quartus 20.1 install path!

🔇 Installing ModelSim - Intel FPGA Edition or Starter Edition Model Technology ModelSim - Intel F 🚽	ο×
Ready to Install	(intel)
Summary: Installation directory: Dr.Vetal/PGA_litet20.1 Required disk space: 320276 MB Available disk space: 320276 MB	
InstallBuilder	Cancel

Last step, before the install begins.

# 1.2 USB BLASTER DRIVER, INSTALL AND CHECK

\*\*Note\*\*, if the USB Blaster is not installed properly, you won't be able to Program your DE10-Lite board!

The USB Blaster driver **is included** in the download for the Quratus Prime itself. Verify that you do have a folder by the name **usb-blaster-ii** under this path, where text in blue is, *as per your own unique case*.

your\_drive:\intelFPGA\_Lite\20.1\quartus\drivers

If run into trouble with your USB driver and are having trouble communicating with the Board, check these instructions:

https://www.terasic.com.tw/wiki/Altera\_USB\_Blaster\_Driver\_Installation\_Instructions

https://mil.ufl.edu/3701/docs/quartus/byteblaster/usb-blaster\_driver\_install.pdf

# 1.3 TEST QUARTUS INSTALL AND USE THE IDE

Perform the steps under this section...

- 1) To ensure that your SW installation went fine and
- 2) Get familiar in using Quartus IDE, for doing your labs. Having the Quartus Prime SW, user guide handy, would be useful.

This section **assumes** that you have successfully installed Quartus SW, Max 10 device support files and the USB Blaster driver.

#### 1.3.1 NEW PROJECT WIZARD

Start Quartus SW, from the desktop shortcut or from Windows Start menu.

1. Open a New Project Wizard, by selecting *File -> New Project Wizard* 

You would see the following screen..

2	New Project Wizard	×				
	Introduction					
	The New Project Wizard helps you create a new project and preliminary project settings, including the following:					
	<ul> <li>Project name and directory</li> <li>Name of the top-level design entity</li> <li>Project files and libraries</li> <li>Target device family and device</li> <li>EDA tool settings</li> </ul>					
	You can change the settings for an existing project and specify additional project-wide settings with the Settings command (Assignments menu). You can use the various pages of the Settings dialog box to add functionality to the project.					
e ; t :						
	Don't show me this introduction again					
	< Back Next > Finish Cancel Help					

Click on 'Next' and you will see the screen shown below....

a (1 +  a - )		ectory for this					_
		20p1/DE10Li	te/StairSw				
	e name of thi	s project?					
ThreeWay							
		e top-level de in the design		his project? This	name is case se	ensitive and mus	t exactly
	entity name i	in the design	me.				_
Light							
Use Existin	ng Project Se	ettings					
	<b>S</b>		Quartus F	Prime	×		
			MyProjects/Qua t. Do you want t	rtus20p1/DE10 o create it?	Lite/StairSw"		
				Yes	No		

On this window, fill out...

- a) The path and the name of the directory, where you want the project to be created and stored.
- b) The name of your project
  c) The name of the Top Level module, in your Project. It is **important** that the name is entered exactly, including the case, as it in your code, so that it matches.

If the working directory is not existing, you will get a message, asking for your permission to create the directory. Click Yes and then go to the next screen, by clicking Next.

3	New Project Wizard ×
ł	Project Type
S	Select the type of project to create.
(	Empty project
	Create new project by specifying project files and libraries, target device family and device, and EDA tool settings.
(	O Project template
	the Quartus Prime software, or download design templates from the <u>Design Store</u> .
	< Back Next > Finish Cancel Help

Use the default *Empty Project* setting and click Next. This takes you to the tab, for adding files, to your project.

New Project Wizard		×
Add Files		
Select the design files you want to include in the project. Click Add All to add all des directory to the project.	ign files in th	ne project
Note: you can always add design files to the project later.	rowse to you	ır files
File name:		Add
٩,	×	Add All
File Name Type Library Design Entry/Synthesis Tool HDL Version		Remove
		Up
		Down
		Properties
Specify the path names of any non-default libraries. User Libraries		
	Consol	
< Back Next > Finish	Cancel	Help

For the time being, we won't add files here, in this step. Note, you can always add files to the project, later also. Click Next, to proceed to wizards' next step.

Device Board									
Select the family and d You can install additior			and on the To	ools menu.					
To determine the versi	on of the Quartus Pri	re in which your 1	arget device	is supported, refer to	the Device Suppor	t List webp	age.		
Device family				-	Show in 'Available	e devices' list		-	
		_			onon in Aranabic				
Family: MAX 10 (DA)				-	Package:	FBGA			-
Device: MAX 10 D/	A			-	Pin count:	484			-
Target device					Core speed grade	: 7			•
Auto device select	and builded Fierra				Name filter:				
	2								
Specific device se	lected in 'Available de	vices' list			Show advanced devices				
Other: n/a									
Other: n/a									
Other: n/a Available devices:									
	Core Voltage	LES	Total I/Os	GPIOs	Memory Bits	d multiplier 9-bit	PLLs	Global Clocks	Maximu ^
Available devices:	Core Voltage	LEs	Total I/Os 320	GPIOs 320	Memory Bits 562176	<b>d multiplier 9-bit</b> 90	PLLs 4	Global Clocks	Maximu ^
Available devices: Name	_				-				
Available devices: Name 10M16DAF484I7P	1.2V	15840	320	320	562176	90	4	20	4587520
Available devices: Name 10M16DAF484I7P 10M25DAF484A7G	1.2V 1.2V	15840 24960	320 360	320 360	562176 691200	90 110	4 4	20 20	4587520 6291456
Available devices: Name 10M16DAF48417P 10M25DAF484A7G 10M25DAF484C7G	1.2V 1.2V 1.2V	15840 24960 24960	320 360 360	320 360 360	562176 691200 691200	90 110 110	4 4 4	20 20 20	4587520 6291456 6291456
Available devices: Name 10M16DAF484I7P 10M25DAF484A7G 10M25DAF484C7G 10M25DAF484I7G	1.2V 1.2V 1.2V 1.2V	15840 24960 24960 24960	320 360 360 360	320 360 360 360	562176 691200 691200 691200	90 110 110 110	4 4 4 4	20 20 20 20	4587520 6291456 6291456 6291456
Available devices: Name 10M16DAF48417P 10M25DAF484A7G 10M25DAF484C7G 10M25DAF48417G 10M40DAF484C7G	1.2V 1.2V 1.2V 1.2V 1.2V	15840 24960 24960 24960 40368	320 360 360 360 360	320 360 360 360 360 360	562176 691200 691200 691200 691200 1290240	90 110 110 110 250	4 4 4 4 4	20 20 20 20 20 20	4587520 6291456 6291456 6291456 11534336
Name           10M16DAF48417P           10M25DAF484A7G           10M25DAF484A7G           10M25DAF48447G           10M40DAF48417G           10M40DAF48417G           10M40DAF48417G           10M50DAF48417G           10M50DAF48417G	1.2V 1.2V 1.2V 1.2V 1.2V 1.2V 1.2V	15840 24960 24960 24960 40368 40368	320 360 360 360 360 360 360 360 360	320 360 360 360 360 360 360 360 360	562176 691200 691200 691200 1290240 1290240	90 110 110 250 250 288 288	4 4 4 4 4 4 4 4 4	20 20 20 20 20 20 20 20 20 20	4587520 6291456 6291456 6291456 11534336 11534336
Available devices: Name 10M15DAF48417P 10M25DAF484A7G 10M25DAF48447G 10M25DAF48417G 10M40DAF48417G 10M40DAF48417G 10M50DAF48417G 10M50DAF48417F	1.2V 1.2V 1.2V 1.2V 1.2V 1.2V 1.2V 1.2V	15840 24960 24960 24960 40368 40368 40368	320 360 360 360 360 360 360 360	320 360 360 360 360 360 360	562176 691200 691200 691200 1290240 1290240 1677312	90 110 110 110 250 250 288	4 4 4 4 4 4 4 4 4	20 20 20 20 20 20 20 20 20 20	4587520 6291456 6291456 6291456 11534336 11534336 11534336 11534336
Name           10M16DAF48417P           10M25DAF484A7G           10M25DAF484A7G           10M25DAF48447G           10M40DAF48417G           10M40DAF48417G           10M40DAF48417G           10M50DAF48417G           10M50DAF48417G	1.2V 1.2V 1.2V 1.2V 1.2V 1.2V 1.2V 1.2V	15840         24960         24960         24960         40368         40368         40368         49760	320 360 360 360 360 360 360 360 360	320 360 360 360 360 360 360 360 360	562176 691200 691200 1290240 1290240 1677312	90 110 110 250 250 288 288	4 4 4 4 4 4 4 4 4	20 20 20 20 20 20 20 20 20 20	4587520 6291456 6291456 6291456 11534336 11534336 11534336 11534336

This is an important tab. For DE10-Lite board, fill out as shown above and click Next.

🕤 New Project Wizard			ww.Sinnuconac.qp)	×		
EDA Tool Settir	ngs					
Specify the other EDA tools used with the Quartus Prime software to develop your project.						
EDA tools:						
Tool Type	Tool Name	Format(s)	Run Tool Automatically			
Design Entry/Synth	<none> 🔻</none>	<none> 👻</none>	Run this tool automatically to synthesize the current design			
Simulation	ModelSim-Altera 🔹	Verilog HDL 🔻	Run gate-level simulation automatically after compilation			
Board-Level	Timing	<none> 🔻</none>				
	Symbol	<none> •</none>				
	Signal Integrity	<none> •</none>				
	Boundary Scan	<none></none>				

In the EDA Tool Settings window, select 'ModelSim-Altera' as the Tool and Verilog-HDL as the Format.

oc	S New Pro	iect Wizard	×
	Summary		
:hy	When you click Finish, the project will be created with the following settings:		
	Project directory: Project name: Top-level design entity: Number of files added: Number of user libraries added:	C/MyProjects/Quartus20p1/DE10Lite/StairSw ThreeWaySw Light 0 0	
	Device assignments: Design template: Family name: Device: Board:	n/a MAX 10 (DA/DF/DC/SA/SC) 10M50DAF484C7G n/a	
nir er)	EDA tools: Design entry/synthesis: Simulation: Timing analysis: Operating conditions:	<none> (<none>) <none> (<none>) 0</none></none></none></none>	
	Core voltage: Junction temperature range:	1.2V 0-85 °C	
		< Back Next > Finish Cancel Help	

Do the same for this last slide and click Finish.

#### 1.3.2 ADDING FILES

After you have done the above steps, Quartus would show you a view like below, showing only your Top level Module, as you declared it in the previous steps, since no files and lower hierarchy modules are currently present.

<b>3</b>		Quartus Prime Lite Edition - C:/MyProjects/Quartus20p1/DE10Lite/StairSw/ThreeWaySw - Light
File Edit View Project	Assignments Processing Tools Window	Help
□ ► ■ ≠ □ ■ □ ○ ○	Light 🔹 🖌 🎸 🎸 🗸	○ ▷ ► ► K ♀ ◎ A ≫ B ●
Project Navigator	🔺 Hierarchy 🔹 🕅 🖉 🗧 🗙	
	Entity:Instance	
<ul> <li>MAX 10: 10M50DAF484C</li> <li>Light <sup>A</sup></li> </ul>	7G Name of your Top Level Module	
<	>	
Tasks	Compilation • = 💷 8 ×	
	Task Time	
4 🕨 Compile Design		

To add the files, you would do the following steps...

<b>S</b>			Quartus Pr	ime Lite Editi	ion - C:/My	MyProjects/Quartus20p1/DE10Lite/StairSw/ThreeWaySw - Light
File Edit View Pr	oject Assignments Processing	Tools Window	Help			
0 🗖 🖬 🗲 🗅 🗈	つで Light	- 180	0 F F K Q	🛛 🕹 🌺 🔝	•	
Project Navigator	Files	- 1				
Fil						
Add/Remov	ve Files in Project					
Tasks	Compilation	• ≡ <b>0</b> 8 ×				
	Task	Time				
🔺 🕨 Compile I						
	sis & Synthesis					
	Place & Route)					Quartus Prime
	bler (Generate programming files)					
🛛 🕨 🏲 Timing						
🖻 🕨 EDA N						
Edit Settin						
Program	Device (Open Programmer)					
<		>				
х в All 🛛 🛆	▲ × < <filter>&gt;</filter>		💏 Find	# Find Next		
9						
= Tvbe ID M	lessade					

Select Files from the drop down menu. *Right click* on the 'Files' under the Project Navigator and select 'Add/Remove Files in Project'

Category:		Device/Bo	ard.
General	Files		
Files	Select the design files you want to include in the pr	oiect. Click Add All to add all design files in the	
Libraries	project directory to the project.	Click, to browse for your file	15
<ul> <li>IP Settings</li> </ul>		$\sim$	
IP Catalog Search Locations	File name:	Add	
Design Templates 4 Operating Settings and Conditic	•	X Add All	
<ul> <li>Operating Settings and Conditic Voltage</li> </ul>	File Name Type Library Design Entry/Synthesis	Tool HDL Version Remove	
Temperature			
Compilation Process Settings		Select File	
Incremental Compilation	(e) → 1 ↓ « MyProjects + Quartus2	0p1 → DE10Lite → StairSw → V C	Search StairSw P
EDA Tool Settings Design Entry/Synthesis			
Simulation	Organize • New folder		li • 🔟 🔞
Board-Level	★ Favorites	▲ Name ▲	Date modified Ty
Compiler Settings		L db	2020-12-17 11:58 Fil
VHDL Input	No Homegroup	✓ Lighty	2020-12-17 12:46 V Prime
Verilog HDL Input	in the state of th	Ugntv	2020-12-17 12:46 V
Default Parameters Timing Analyzer	IN This PC		sion 20.1 Lite Editi
Assembler	Desktop		
Design Assistant			
Signal Tap Logic Analyzer	Documents		
Logic Analyzer Interface	Downloads		
Power Analyzer Settings	Music		
SSN Analyzer	Pictures		
	Videos		
	Section 2015 Windows (C:)		
	🥪 KINGSTON (D:)	~ <	
		Ψ. (	
· · · · · · · · · · · · · · · · · · ·	File name: Light.v		✓ Design Files (*.tdf *.vhd *.vhr ✓
			Open Cancel
Type ID Message			
<			
System Processing			

Browse to the directory which contains your HDL (Verilog, VHDL, SystemVerilog) file. In the case shown a Verilog file called Light.v is visible. This file was previously created and saved under the project directory.

Here is the sample code in this file (Credit: Altera document 'Quartus II Introduction Using Verilog Design'). Using a texteditor of your choice, you can copy and save this file, under the directory, from where you want to import it, preferably your project directory, into your project. (Pay attention to the name of the module!)

```
module Light (x1, x2, f);
input x1, x2;
output f;
assign f = (x1 & ~x2) | (~x1 & x2);
endmodule
```

This is design of a simple two-way light controller, which we typically find in our homes, on stairs. Below is the diagram and Truth table of this circuit.

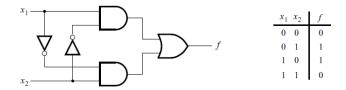
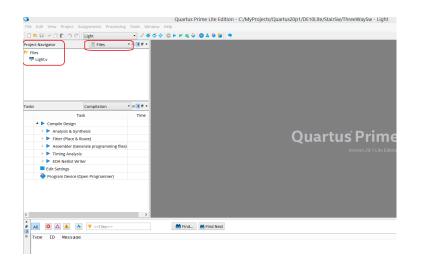


Figure 12. The light controller circuit.

When you click 'open' on the last picture shown above, and then click 'Add', you see the following window... \*\*Note\*\*, you can open multiple files, in one go. In that case, click on 'Add All', so that they get added to the project.

ategory:							Device/Board	01/DE10Lite/StairSw/ThreeWaySw - Light
General	Files							
Files	Select the design	n files you want to in	clude in :	the project. Click Add	d All to add	l all design fi	les in the	
Libraries	project directory							
IP Settings								
IP Catalog Search Locations	File name:						Add	
Design Templates	۹.					×	Add All	
Voltage	File Name	Type	Library	Design Entry/Synth	esis Tool	HDL Versio	Remove	
Temperature	Lighty	Verilog HDL File		<none></none>		Default		
<ul> <li>Compilation Process Settings Incremental Compilation</li> </ul>	cigitat	Terrog Hoe The					Up	
EDA Tool Settings	l						Down	
Design Entry/Synthesis							Properties	
Simulation								
Board+Level								
Compiler Settings								
VHDL Input								Quartus Primo
Verilog HDL Input								
Default Parameters								Version 20.1 Lite Edit
Timing Analyzer								Version 20.1 Ere Eur
Assembler								
Design Assistant								
Signal Tap Logic Analyzer								
Logic Analyzer Interface Power Analyzer Settings								
SSN Analyzer Settings								
SSN Analyzer								
	<					>		
		W Buy S	- (+	ОК	Cancel	Apply	Help	
< >>		in buy 3						a

Click ok and the file/s are added to the project. When we do it, the following screen is seen and you see that our file Lights.v has been added to the project.



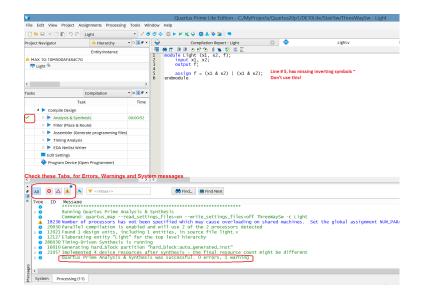
#### 1.3.3 COMPILING THE DESIGN

After we have added the file/s the next step is to compile the design, fix any errors, look at the warnings and preparing the design, for checking / testing on the board.

Right click on the 'Analysis & Synthesis' step, under the Compile Design options, and select Start.

<b>S</b>			Quartus Prime Lite Edition	n - C:/MyProjects/Quartus20p1/DE10Lite/StairSw/ThreeWaySw - Light
File Edit View Project	Assignments Processing	Tools Window He	lp	
🗋 🖿 🖶 🗠 🗇 💼 🗇 C	Light	- / 6 6 6 6	D 🕨 🖌 K 🗢 🔕 A 🔌 🙀 🗢	
Project Navigator	A Hierarchy	• • • • • • • • • • • • • • • • • • •		
MAX 10: 10M50DAF484C	Entity:Instance			
<		>		
Tasks	Compilation	* = 📮 Ø ×		
т	ask	Time		
4 🕨 Compile Design				
Analysis & Com	nthacle			
Fitter (Place)	Start			Quartus Prime
Assembler	Start Again			
🕒 🕨 Timing Ani	Stop Processing C	trl+Shift+C		
🖻 🕨 EDA Netlis	Edit Settings			
Edit Settings	View Report			
Program Devi	Expand All Collapse All			
	Edit Flow			
	New Flow			
<		>		
* <b>6</b> All <b>0</b> 🛆 <b>1</b>	<pre>&lt;<filter>&gt;</filter></pre>		💏 Find 💏 Find Next	
Type ID Messad	e			
sa s				
System Processing				
2 -,				

After the compilation step is complete, if there are any errors, fix them. Also closely look at the error and warning messages, as they often provide good clues to where the problem / potential problems lie in your code.



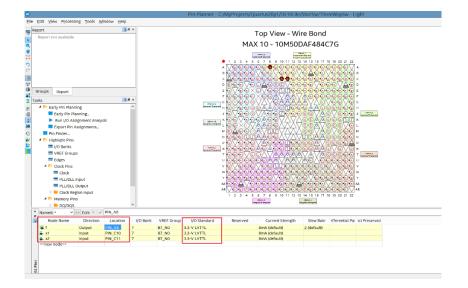
After the compile result is satisfactory, the next step usually is to *lock the Pins* (aka assigning the input, output ports of the design, to specific pins of the FPGA chip), so that the design, when ready can be tested on the board. This simple design only has three ports, so please assign manually, as shown in the picture below.

\*\***Note**\*\*, when the design has many ports, it is often fasters and less error-prone, to '*import*' the pin assignments. How to do this shall be explained later, in more detail. For now, manually assign the ports x, y and f, to the pins, as shown below.

First, open the Pin Planner tool, as shown.

									Quartus Prime Lite Edition - C:/MyProjects/Quartus20p1/DE10Lite/StairSw/ThreeWaySw - Light
Eile	<u>E</u> dit	<u>V</u> iew	Project	As	signments Processing	<u>z T</u> ools	<u>W</u> ir	ndow <u>H</u> elp	
i r	<b>b</b>	40	00	٠	Device				KK Ó Ø T Ø B 🖕
Pro	ect Navi	gator		2	Settings		C	trl+Shift+E	Compilation Report - Light 🛛 🧇 Light.v
				4	Assignment Editor		c	trl+Shift+A	
	MAX 10:	10M5	0DAF484	ø	Pi <u>n</u> Planner		c	trl+Shift+N	e Light (x1, x2, f); nput x1, x2;
	Light				Bemove Assignments				utput f;
				13	Back-Annotate Assign				ssign f = (x1 & x2)   (x1 & x2);
_					Import Assignments				dule
<					Export Assignments				
Tas	ks				Assignment Groups				
				۵	Logic Lock Regions W	/indow	A	lt+L	
	4 🕨	Comp	ile Desigr	÷	Design Partitions Win	ndow	A	lt+D	
-	Þ	► An	alysis & S	ynth	esis	00:00:52			
	Þ	Fit	ter (Place	& R0	oute)				
	Þ	As:	sembler (	Sene	rate programming files	5)			
	Þ	Tir	ning Anal	ysis					
	Þ	ED	A Netlist	Write	er				
		Edit Se	ettings						
	۵	Progr	am Devio	e (Op	en Programmer)				
<							>	<	
×		8			▼ < <filter>&gt;</filter>				💏 Find 👩 Find Next
<b>6</b> 4	All	•	<u>a</u>	~	< <filter>&gt;</filter>				Tind of Find Next
=	Type	ID	Messa	ae					
	•	1823	6 Numbe	r o	f processors has	s not be	en	specifie	ed which may cause overloading on shared machines. Set the global assignment $NUM_P$

Then in the Pin Planner tool, manually assign the pin locations, to the three ports.



After this step, close the Pin Planner tool and then we will do a complete Compile Step on our design. Once the compile step is successfully done, you would see green check marks, next to the four main steps of the design compile process, as shown below.

🗋 🗖 🖯 🖗 🖉 🗂 👘 🔊	C" Light	- / 4	5 4 4 9 F F K 🕂 🛛 A 🕉 🗃 🖕				
oject Navigator	A tilerarchy	• 0 <b>12</b> 0 •			Lightw		
	Entity/instance		Table of Contents	Row Summary			
MAX 10: 10MS0DAF40	4076		III Flow Summary	A + Filter >>			
👎 Ueht 🏝			I Flow Settings	Row Status	Successful - Thu Dec 17 13:2	639 2020	
-			Flow Non-Default Global Settings	Quartus Prime Version	20.1.0 Build 711 06/05/2020	SJ Lite Edition	
		>	Flow Elapsed Time	Revision Name	Light		
sks	Compilation	• = <b>3</b> .0 ×	Flow OS Summary	Top-level Entity Name	Light		
945		_	E Flow Log	Family	MAX 10		
-	Task Right click on 'Compile	Time	Analysis & Synthesis     Enter	Device	10M50DAF484C7G		
🖌 🕈 🕨 Compile Desig	Right click on 'Compile Design' and select Start	00:03:20	Fine      Fine	Timing Models	Final		
🔹 🕨 🕨 Analysis A	Synthesis	00:00:48	Plow Pressages     Plow Suppressed Messages	Total logic elements Total registers	2 / 49,760 ( < 1 %)		
🔹 🕨 🕨 Fitter (Flace	e & Route)	00:00:58	<ul> <li>Assembler</li> </ul>	Total registers	0 3/360(11%)		
Assembler	(Generate programming the	9 00:00:56	E Timing Analyzer	Total virtual pins	57300(5136)		
Timing And	vlysis	00:00:38	Since no clocks and not clock timing	Total memory bits	0/1677312(0%)		
🕨 🕨 EDA Netlist	t Wilter		info was used. Thus ok to ignore.	Embedded Multiplier 9-bit elements			
Edit Settings				Total PLLs	0/4(0%)		
Program Devis	ce (Open Programmer)			UFM blocks	0/1(0%)		
To multch hotseon	Warnings, Errors and Sys	70m >	< >	ADC blocks	0/2(0%)		
		AVIII					
All 🖸 🔬 🔺	★ < <filter>&gt;</filter>		💏 Find., 😸 Find Next				
Type ID Mess	309						
▲ 18236 Numb	en of processors has	s not beer	n specified which may cause overloading o	on shared machines. Set th	e global assignment N	UN PARALLEL PROCESSORS in	your QSF to an appropriate vi
▲ 18236 Numbe	er of processors has	s not beer	i specified which may cause overloading ( ble with a valid subscription license. W	on shared machines. Set th	e global assignment N	UN_PARALLEL_PROCESSORS in	your QSE to an appropriate va
A 15714 Some	pins have incomplet	te 1/0 as:	signments. Refer to the L/O Assignment W	arnings report for details			
			file not found: 'Light.sdc'. A Synopsys	Design Constraints File is	required by the Timir	ng Analyzer to get proper	timing constraints. Without
	locks defined in de		irements for 3.3-, 3.0-, and 2.5-V inter	forer for more information	notion to AN AAT: TH	terfacing MAX 10 Devices a	d+b 2 2/2 0/2 5 V 1VTD /1VOM
	er of processors has	s not beer	a specified which may cause overloading (	on shared machines. Set th	e global assignment N	UN_PARALLEL_PROCESSORS in	your OSF to an appropriate va
18236 Numbe	er of processors has	s not beer	a specified which may cause overloading a	on shared machines. Set th	e global assignment N	UN_PARALLEL_PROCESSORS 1n	your QSF to an appropriate v
▲ 18236 Numbe	psys Design Constra	ints File	file not found: 'Light.sdc'. A Symopsys	Design Constraints File is	required by the Timi	ng Analyzer to get proper	timing constraints. Without
▲ 18236 Numb ▲ 18236 Numb ▲ 332012 Synot	locks defined in de						
▲ 18236 Numb ▲ 18236 Numb ▲ 332012 Syno ▲ 332068 No. c			Warning messages, in Blue				
▲ 18236 Numbe ▲ 18236 Numbe ▲ 332012 Symon ▲ 332068 No. c ▲ 332068 No. c	locks defined in de						
▲ 18236 Numb ▲ 18236 Numb ▲ 332012 Synop ▲ 332068 No c ▲ 332068 No c							
▲ 18236 Numbe ▲ 18236 Numbe ▲ 332012 Symon ▲ 332068 No. c ▲ 332068 No. c							
▲ 18236 Numb ▲ 18236 Numb ▲ 332012 Synop ▲ 332068 No c ▲ 332068 No c	locks defined in de						

You may notice, that the Timing Analyzer is in red. This is because we do not have any clocks in our design and as such no clock timing information was used. This can be safely ignored.

#### 1.3.4 PROGRAMMING THE BOARD

After the compile step is over, it is time to program the board and test the design on the board. For this we need to use the Programmer tool.

\*\*Note\*\*, Before attempting this step, the DE10-Lite board should already be connected to your laptop, via the USB cable. When the board is powered up, the Hex displays shows numbers between 0 and F, while the LEDS blink on and off, in a rotoary form.

Do menu Tools -> Programmer (or click on the Progammer icon) and you would see the following window.

Enable real-	time ISP to allow back		ming when		Mode: JTA	5		•	Proj	gress:		
⊮ <sup>n</sup> ® Start	File	Device	Checksum	Usercode	Program/ Configure	Verify	Blank- Check	Examine	Security Bit	Erase	ISP CLAMF	
™u Stop	output_files/Light	10M50DAF484	0026FDF3	0026FDF3	~							
Auto Detec 🗙 Delete		<b>&gt;</b>				Н	ardwar	e Setup	1			×
📥 Add File			Hardware S	ettings	JTAG Settine	25						
<sup>D</sup> Change File					hardware set		use whe	n program	ming dev	ices. Tł	nis programr	ning
🛱 Save File	(intel)	ie 📕 .	hardware se	tup applies	s only to the	currer	nt progra	mmer win	dow.			
Add Device			Currently se		lware: No I	Hardw	are					•
1 <sup>th</sup> Up	10M50DAF	-	Hardware fr Available h	equency: nardware it	ems							Hz
+ " Down	+		Hardware		Ser		Port				Add Hard	lware
<sup>↓¶</sup> Down			USB-Blast	ter	Loci	al	USB-0				Remove Ha	ardware
≑ ¤ Down			4									
+ ¤ Down			00000		SB-Blaster a d hardware		will bec	ome the				

#### Make sure, that Mode is JTAG!

Initially under Hardware Setup, you may see 'No Hardware'. If this is the case, double click on Hardware Setup, to open it's window. If your USB Blaster driver was installed properly, you will see USB-Blaster available. Double click on it, so it becomes the 'currently selected hardware' and then Close the window.

You should now be back into the Programmer Tool, with USB-Blaster now visible, as shown below.

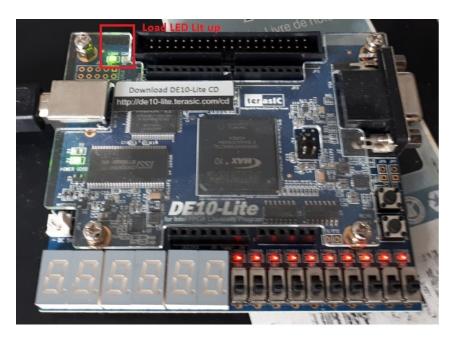
Eile Edit View	Processing Tools	s <u>W</u> indow <u>H</u> e	p								Search	altera.cor	n
🚣 Hardware S	etup USB-Blaster [	[USB-0]			Mode: JTA	G			Prog	ress: [			
Enable real-	ime ISP to allow back	ground program	ming when	available								on of progra een bar he	
M Start	File	Device	Checksum	Usercode	Program/ Configure	Verify	Blank- Check	Examine	Security Bit		ISP CLAMF		
II <sup>®</sup> Stop	output_files/Light	10M50DAF484	0026FDF3	0026FDF3	<ul><li>✓</li></ul>	]							
🏓 Auto Detec													
× Delete													
찬 Add File													
° Change File													
🖺 Save File													
Add Device													
t <sup>%</sup> ⊔ Up													
It Down	TDO 10M50DAF	484											

Make sure, Program / Configure is checked off, next to your SOF file.

\*\*Note\*\*, if you don't see the SOF file automatically selected, click on 'Add File' and browse your project's Output directory and select your SOF file, so that it gets added to the Programmer.

Click Start and programming of your board shall starts. If everything went well, the Progress bar should get completely full with a green bar.

During programming, you will see that the 'Load' LED on the board lights up, as shown below.



Board being Programmed.

## 1.3.5 TESTING DESIGN ON BOARD

This design is a simple two-switch controller, commonly seen around stairways. The X and Y inputs are the switches SW1 and SW0, while the F output is going LEDR0.

When the design is working properly, you will notice results, as shown below.



X is on, Y is off. The Light is on.

Both X and Y are on, the Light is off.

By completing these steps, you have verified your setup and are now ready for your Labs!

#### 1.3.6 A SMALL TWEAK

You would have noticed that in the pictures above, the 9 LEDs to the left of LEDR0 are also dimly lit up.

If want to correct this, go to menu Assignments -> Device

Then follow the steps, as outlined in the picture below. Apply these changes. Re-compile and re-program your design and now those un-used LEDs won't light up.

Device       Based         Select family and device you want to arget for complexity of the insuit Devices command on the Tools menu.       Device and Pin Options - Light         To determine the version of the Quarture Prime software in which your target device is supported, refer to the Device.       Select family         Device and Pin Options - Light       Comparison in Valiable devices         Device and Pin Options - Light       Comparison in Valiable devices         Device and Pin Options - Light       Device and Pin Options - Light         Device and Pin Options - Light       Comparison in Valiable devices         Device and Pin Options - Light       Device and Pin Options - Light         Device and Pin Options - Light       Device and Pin Options - Light         Device and Pin Options - Light       Device and Pin Options - Light         Device and Pin Options - Light       Device and Pin Options - Light         Device and Pin Options - Light       Device and Pin Options - Light         Device and Pin Options - Light       Device and Pin Options - Light         Device and Pin Options - Light       Device and Pin Options - Light         Device and Pin Options - Light       Device and Pin Options - Light         Device and Pin Options - Light       Device and Pin Options - Light         Device and Pin Options - Light       Device and Pin Options - Light         Device and Pin Options - Light	2					Device	2	
Orace and Entry Option and existing autoport with the install devices command on the Tools menu.         Centre and Entry Option Security         Centre an	Device Board							
Device family     Show in Available devices     Show in Available devices     General     Outcode family       Parkies devices devices devices devices devices for the family device.     Processed grade     Processed grade     Processed grade       Name files:     Processed grade     Processed grade     Processed grade     Processed grade       Octors:     Processed grade     Processed grade     Processed grade     Processed grade       Obstract     Processed grade     Processed grade     Processed grade     Processed grade       Obstract     Processed grade     Processed grade     Processed grade     Processed grade       Name files:     Processed grade     Processed grade     Processed grade     Processed grade       Obstract     Processed grade     Processed grade     Processed grade     Processed grade       Obstract     Processed grade     Processed grade     Processed grade     Processed grade       Voltage     Processed grade     Processed grade     Processed grade     Processed grade       Processed grade     Specify devices devices     Processed grade     Processed grade     Processed grade       Name files:     Total V/Os     Brode total grade     Processed grade     Processed grade       Processed grade     Specify devices devices     Processed grade     Processed grade					ommand on th	ne Tools menu	ı.	Device and Pin Options - Light
Decice family         Show in Available devices         Show in Available devices         Configuration         Configuration         Configuration         Specify device-wide options for reserving all unused pins on the device. To reserve individual of Available devices         Specify device-wide options for reserving all unused pins on the device. To reserve individual of Available devices         Specify device-wide options for reserving all unused pins on the device. To reserve individual of Change to this           Auro device selected in Available devices         Berker all Propose Pins         Specify device-wide options for reserving all unused pins. A input triated         Configuration           Vision         Others: n/a         Device all Propose Pins         Construct of the Available devices         Construct of the Avainport of the Available devices         Const	o determine the ver	rsion of the Quartu	s Prime so	ftware in which y	our target de	vice is suppor	ted, refer to the <u>Device Su</u>	
Family:         MAX 10 (DA/0F/DC/SA/SO         •         Processent and the second se	Device family					s	how in 'Available devices' l	
Device All         Prin count:         B44         Durit August Print Print         Print count:         B44           Target device         Core speed grade 7         Print count:         B4         Durit August Print Print Print         Durit August Print	Family: MAX 10 (D	A/DF/DC/SA/SC)				• p	ackage: FBGA	Specify device-wide options for reserving all unused pins on the device. To reserve individual dual- purpose configuration pins, go to the Dual-Purpose Pins tab. To reserve other pins individually, use
arget device       Core speed grade 7       And device selected in Vanilable devices list       Core speed grade 7       Core speed grade 7       Core voltage       Core	Device: All					۳P	in count: 484	Assignment Editor.
Name         Core Voltage         LE         Total I/Os         G/IO         Memory Bits         Embedded memory Bits         Memory Bits         Embedded memory Bits         Memory Bits <t< td=""><td>Auto device sel     Specific device :</td><td colspan="5">Name filter: Name filter Name filter: Specific device selected by the filter Specific device selected in Available devices' list Cl Show advanced device Device and Pin Options.</td><td>lame filter:</td><th>4 Change to this As input tri-stated with bus-hold dirouitry As input tri-stated with weak pull-up As output driving an unspecified signal</th></t<>	Auto device sel     Specific device :	Name filter: Name filter Name filter: Specific device selected by the filter Specific device selected in Available devices' list Cl Show advanced device Device and Pin Options.					lame filter:	4 Change to this As input tri-stated with bus-hold dirouitry As input tri-stated with weak pull-up As output driving an unspecified signal
DM40DAF484C76         1.2V         40368         360         120240         250           DM40DAF484C76         1.2V         40368         360         130240         250           DM40DF484C76         1.2V         40368         360         130240         250           DM40DF484C76         1.2V         40368         360         130240         250           DM40DF484C76         1.2V         40568         360         1607         122           DM40DF484C76         1.2V         40568         360         1607         127         288           DM40DF484C76         1.2V         40760         360         1677312         288         280           DM50DF484D7         1.2V         40760         360         1677312         288         286           DM50DF484D7         1.2V         40760         360         1677312         288         <	vailable devices:							
OM400AF48470         12V         4036         360         1200240         250           OM400AF48470         12V         4036         360         1200240         230           OM400Cr44107         12V         4036         360         1200240         230           OM400Cr44107         12V         40760         360         360         1677312         288           OM500AF48470         12V         40760         360         360         1677312         288           OM500Cr44470         12V         40760         360         1677312         288         Description:           OM500Cr44470         12V         40760         360         1677312         288         Description:		-						
044007244776 12V 4096 300 500 1290240 250 045007448476 12V 40760 360 500 1597312 288 045007448476 12V 40760 360 560 1677312 288 045007448476 12V 40760 360 360 1677312 288 04500748476 12V 40760 360 360 1677312 288 0450074876 12V 40760 360 360 1677312 288 04500748776 12V 40760 360 360 1677312 288 04500748776 12V 40760 360 16778776 12V 40760 400000000000000000000000000000000								
MSD0AF4847C6         1.2V         49760         560         360         1677312         280           MSD0AF4847C6         1.2V         49760         560         360         1677312         280           MSD0AF4847C6         1.2V         49760         360         1677312         280           MSD0F4847C6         1.2V         49760         360         1677312         280								
MS00AF484170         1.2v         49760         360         360         1677312         288           MS00AF484179         1.2v         49760         360         360         1677312         288           MS00AF484176         1.2v         49760         360         360         1677312         288           MS00CF484176         1.2v         49760         360         1677312         288	M40DCF48417G	1.2V	40368	360	360	1290240	250	
MSD0AF48407P         1.2v         49760         560         360         1677312         286           MSD0AF48407G         1.2v         49760         360         1677312         286           MSD0AF48407G         1.2v         49760         360         1677312         286           MSD0AF48407G         1.2v         49760         360         1677312         288           MSD0F48407G         1.2v         49760         360         1677312         288	M50DAF484C7G	1.2V	49760	360	360	1677312	288	
MSDDCF484C7G         1.2V         49760         360         360         1677312         288           MSDDCF48417G         1.2V         49760         360         1677312         288	M50DAF484I7G	1.2V	49760	360	360	1677312	288	
Reserves all unused pins on the target device in one of 5 states: as inputs that are tri-stated, as BGBOC5484776 1.2 43760 360 360 1677312 288 that drive ground, as outputs that are an unspecified signal, as input tri-stated with bus-hold input tri-stated with wesk pull-up.	M50DAF484I7P	1.2V	49760	360	360	1677312	288	
that drive ground, as outputs that affine an unspecified signal, as input tri-stated with bus-hold input tri-stated with weak pull-up.	M50DCF484C7G	1.2V	49760	360	360	1677312	288	Description:
igration Devices O migration devices selected					360	1677312	288	Reserves all unused pins on the target device in one of 5 states: as inputs that are tri-stated, as out that drive ground, as outputs that drive an unspecified signal, as input tri-stated with bus-hold, or input tri-stated with weak pull-up.
s	igration bevices	o migration devic	is selected	1				5 Re
OK Cancel								OK Cancel

# **1.4 OTHER USEFUL LINKS**

This is Intel's **User forum**, which includes useful info on the FPGA related matters too. You can post your issues and search for previously posted / resolved similar issues.

1. https://community.intel.com/

You will be required to Register, to use if fully.

# 2 INSTRUCTIONS FOR THE MACOS SYSTEMS

There are few options for running Quartus on a Mac. The steps in the link below have been **tested and tried** during a previous school term and are recommended, with few extra points, as mentioned below.

Prior to following the steps mentioned in the link below, you would require Ubantu Desktop running in Virtualbox.

1. Install VirtualBox from this link https://www.virtualbox.org/

After you complete the install of the Virtual Box, you should **also install** the "VirtualBox Extension pack".

For that, follow instructions on this link: https://www.nakivo.com/blog/how-to-install-virtualbox-extension-pack/

- 2. Then install Ubantu from this link https://ubuntu.com/download/desktop
- 3. Thereafter follow the steps mentioned under this link, however make sure to keep extra 'virtual disk space' as mentioned below.

https://siytek.com/quartus-mac-virtualbox-ubuntu/

However make following changes in these sections

- Sec 3.1 Recommended virtual disk space'

Set the **virtual box disk space to 50GB** to allow enough space for Quartus, *instead of 30GB* in the online link. Additionally, create this space on your MAC itself and **not** on an external hard drive.

- Sec 4. Install Quartus

Download version 20.1 Lite, for Linux (Registration is required)

Make sure you also download and install ModelSim Altera and Max10 device files.

- Thereafter follow sections 5 and 6, as per the link.

After these steps, to verify your setup, follow the steps in Section 1.3 of **this** tutorial, "*Test Quartus Install and Use the IDE*"

If you run into any issues with install or in verifying your setup, report it to this email:

tech@eecs.yorku.ca